MODEL 2760-17

SF RECEIVER

SECTION 662-5071-304

A2760-17-600

ISSUE 1, NOVEMBER 1984

MODEL 2760-17

SF RECEIVER

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1. GENERAL

A. Scope

1.01 This publication provides a complete description of the Model 2760-17 SF RECEIVER plug-in module. Information on its use and applications is also included. This module is used with the Model 2760 Universal Signaling Analyzer mainframe assembly to monitor SF signaling.

1.02 This publication is being reissued to add additional information and to clarify operating procedures. A glossary of terms, abbreviations, and acronyms has been added as an aid to understanding and use.

B. Organization

1.03 The information contained in this publication is organized as follows:

(a) PART 1. GENERAL: Contains information on the scope and organization of this publication and on the module's specific applications.

(b) PART 2. INSTALLATION: Furnishes general installation instructions including unpacking, inspection, internal switch settings and cable connections, if required, and mainframe installation procedures.

(c) PART 3. DESCRIPTION: Provides a basic description of the module's physical characteristics and front panel layout including indicators and switches.

(d) PART 4. OPERATION: Presents detailed information on how to set up and operate the module. Information is included on test connections, signaling parameters, programming, and display interpretation.

(e) PART 5. THEORY OF OPERATION: Contains specific details on the theory of operation and circuit descriptions.

(f) PART 6. MAINTENANCE: Provides service information, general maintenance procedures, and specific alignment instructions.

(g) PART 7. DIAGRAMS: Furnishes functional, interconnection, parts location, and schematic diagrams.

(h) PART 8. ELECTRONIC PARTS LISTS: Provides a list of all electronic parts used in the module.

(i) PART 9. GLOSSARY: Defines the terms, abbreviations, and acronyms used in this publication.

C. Applications

1.04 The Model 2760-17 SF RECEIVER plug-in module is used for testing and analyzing standard North American 2600 Hz SF signaling systems. The module is plugged in to the Model 2760 Universal Signaling Analyzer mainframe assembly. The module is then enabled via front panel controls. Module signaling parameter values may be changed via the mainframe KEYPAD.

1.05 The Model 2760-17 module is able to:

- Monitor SF address (register) signaling
- Monitor SF supervision (line) signaling
- Display signaling information in real time
- Store signaling information for recall and review.

1.06 Monitored signaling parameters include:

- Transmission level
- Timing relationships
- Supervision events
- Pulse speed and percent break.

1.07 The Model 2760-17 module may be instructed to monitor:

- Address signaling only
- Supervision signaling only
- Both address and supervision signaling.

1.08 When assigned as a supervision receiver, the module monitors calls originating on either of the mainframe input ports for both incoming and outgoing calls.

1.09 When assigned as an address-only receiver, the module monitors only calls present on input port L1. Address signaling present on input port L2 is ignored.

1.10 The module detects and decodes the various SF address and/or supervision signals. When first enabled, the module uses preprogrammed signaling parameter values. The operator may re-program these parameter values to suit the test requirements.

1.11 The codes for the detected signaling are stored and displayed by the mainframe on either the A or B DISPLAY as selected. After completion of a call, the signaling sequence may be recalled and reviewed as desired.

2. INSTALLATION

A. General

2.01 This part contains information needed to unpack and install the Model 2760-17 SF RECEIVER module.

B. Unpacking

2.02 Carefully unpack the Model 2760-17 module from its shipping container. All shipping papers should be noted with the date of receipt, filed, and/or forwarded to the accounting department as appropriate. Save the shipping container and packing material in case a return is necessary.

C. Inspection

2.03 The module is carefully inspected, both mechanically and electrically, before shipment. It should be working properly when received. If damage from transit is found, notify the transportation carrier immediately.

D. Internal Switch Settings

2.04 The 2760-17 module internal switches are factory set for:

- Register (address) signaling display mode
- Expected delay-dial operation.

2.05 Figure 1 shows the physical location of the internal switches S1 and S5. Switch S1 is mounted on the Single Frequency Input Board. Switch S5 is mounted on the Digital Interrupt and Interface Board. Table A provides a description of the S5 switch section functions for each position of the switch, either open or closed.

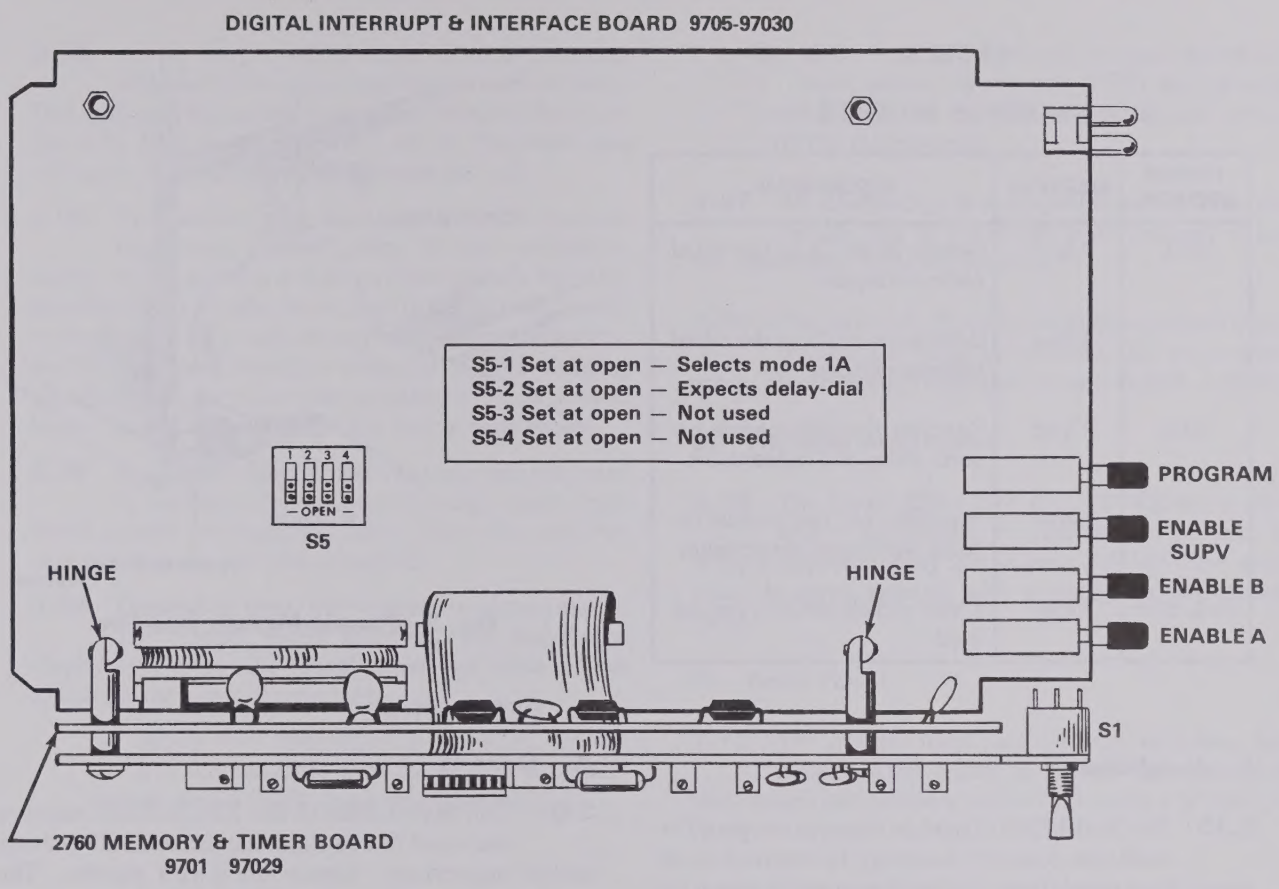
2.06 Switch S1 on the Single Frequency Input Board is used only for special tests during manufacture of the module. Switch S1 is factory set to the OFF position prior to shipment of the module. ***Switch S1 must remain off to ensure proper signal processing and operation of the module.***

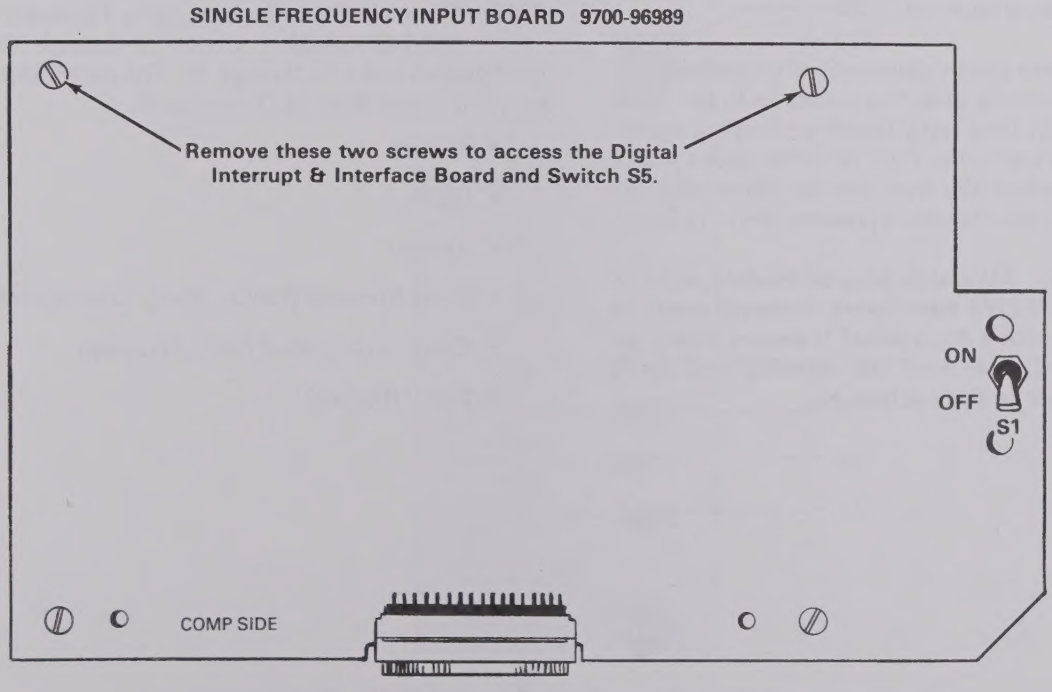
2.07 Switch S5 on the Digital Interrupt and Interface Board selects the register (address) signaling display mode, either 1A or 1B. Switch S5 also sets up the module for either expected delay-dial or wink-start operation. Address signaling display modes (1A and 1B) and delay-dial and wink-start operation are described in PART 4. OPERATION under Programmable Parameters.

2.08 As shown in Table A, section 1 of switch S5 selects address signaling display mode 1A or 1B. Section 2 selects delay-dial or wink-start operation. Sections 3 and 4 are not used and should be in the open position.

2.09 Switch S5 must be correctly set to obtain the desired address signaling display mode 1A or 1B and the expected delay-dial or wink-start operation. To set switch S5 proceed as follows:

STEP	PROCEDURE
1	Make sure S1 is set to the OFF position.
2	Remove the top two screws on the Single Frequency Input Board.
3	Carefully grasp the top edges of the Single Frequency Input and Memory and Timer Boards and gently pull forward. The two boards will swing down on their hinges exposing the Digital Interrupt and Interface Board and switch S5.
4	Set S5 section 1 per Table A for the desired address signaling display mode 1A or 1B.
5	Set S5 section 2 for the expected delay-dial or wink-start operation. The Circuit Layout Record (CLR) card or equivalent document may be referenced to determine the type of circuit operation.
6	Carefully swing the Memory and Timer and Single Frequency Input boards back to their original position.
7	Replace the two top screws on the Single Frequency Input Board. Do not over tighten.




SINGLE FREQUENCY INPUT BOARD 9700-96989
Remove these two screws to access the Digital Interrupt & Interface Board and Switch S5.
ON
OFF
S1
COMP SIDE

C02840-00

Fig. 1—Internal Switch Locations

TABLE A

SWITCH S5 SETTINGS

SWITCH SECTION	POSITION	DESCRIPTION
S5-1	Open	Selects mode 1A as the initial address display.
	Close	Selects mode 1B as the initial address display.
S5-2	Open	Specifies that the module expects delay-dial supervision.
	Close	Specifies that the module expects wink-start supervision.
S5-3, S5-4	Open	These switch sections are not used.

E. Installation

2.10 The Model 2760-17 module requires no special installation. It is only necessary to remove two adjacent dress panels from the mainframe and to insert the plug-in module into the mainframe. The module should then be securely snapped in.

2.11 To ensure proper placement of the plug-in module, carefully slide the module into the mainframe assembly, then apply thumb pressure at a point slightly above and to the right of the module's plastic plunger. Complete the insertion by depressing the plastic plunger into its locked position. Refer to Fig. 2.

Warning: All empty plug-in module jacks in the Model 2760 mainframe assembly must be covered with a dress panel to ensure proper air flow. Failure to heed this warning may result in damage to the equipment.

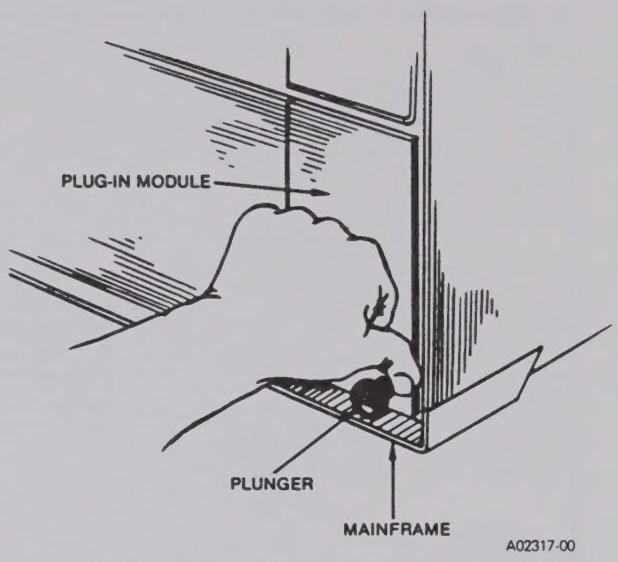


Fig. 2—Plug-in Module Insertion

3. DESCRIPTION

A. General

3.01 The Model 2760-17 SF RECEIVER receives standard North American 2600 Hz SF pulsing and/or supervisory signals on 4-wire circuits. The module is compatible with CCITT R1 line signaling.

3.02 The mainframe displays digits 0 through 9 for address signaling. Digits 11 through 19 are displayed as codes •1 through •9. The mainframe also provides a real-time LED display of:

- Seizure
- Glare
- Answer
- Clear Forward (Calling Party Disconnect)
- Clear Back (Called Party Hang-up)
- Busy (Blocked).

3.03 All of the preceding supervision events plus Idle and Wink (and similar signals such as Delay-Dial or Start-Dial) conditions may be stored by the mainframe for later review on DISPLAY A. The mainframe will store up to 15 supervision events per call.

3.04 The module may be programmed to include numerical violation codes in the mainframe display of SF address and supervision signals violating specified limits for (a) no-tone gap, (b) pulse width, and (c) received level. The module may also be programmed to include numerical violation codes for signals violating specified limits for pulses per seconds (PPS) and percent break. Limits are programmable over a wide range.

3.05 In addition other numerical codes are provided to indicate which pulses in a digit pulse train failed to meet programmed limits. Numerical supervision event codes are also provided.

3.06 Depending upon the register (address) signaling display mode selected, the mainframe display will show the actual measured value of the following signaling parameters:

(a) Mode 1B: The interval between seizure (connect) and the next event, and the interdigital period (IDP), both in milliseconds.

(b) Mode 3: The minimum, average, and maximum pulses per second (PPS) and percent break, and the minimum interdigital period (IDP) in milliseconds.

3.07 All information is displayed in real time as detected, and is recallable from memory using the mainframe's cursor controls.

3.08 The module's dynamic transmission level range is from −40 dBm to +6 dBm (600 ohms reference). The frequency detection criteria is 2600 ± 20 Hz.

B. Physical Description

3.09 The Model 2760-17 SF RECEIVER is a double width (3.0 inches, 76 mm) plug-in module. It weighs approximately 2.5 pounds (1.2 kg). The front panel is spray painted with a semigloss tan enamel finish.

C. Front Panel

3.10 The module front panel layout, switches, and indicators are shown in Fig. 3. The function of each switch and indicator is briefly described in Table B.

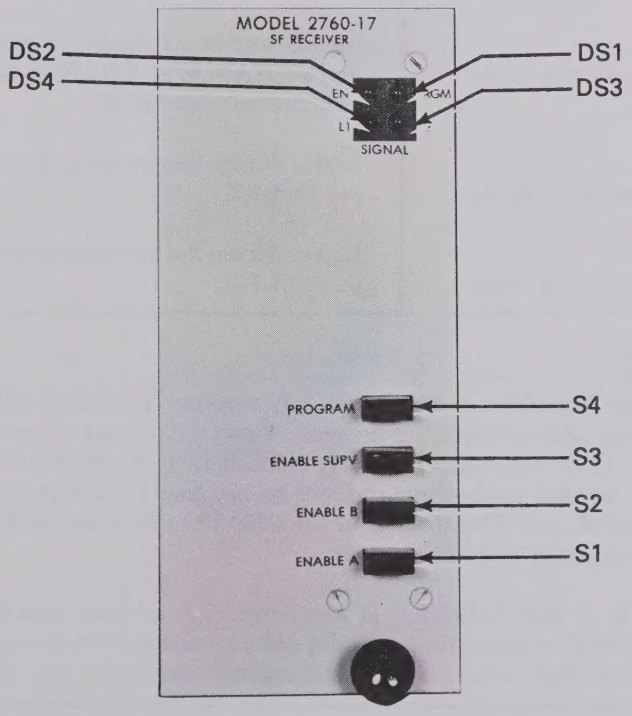


Fig. 3—SF Receiver Front Panel Switches and Indicators

TABLE B

SWITCHES AND INDICATORS

REFERENCE DESIGNATION	NOMENCLATURE	DESCRIPTION
S1	ENABLE A double action pushbutton switch	When depressed, assigns the module as an address (register) signaling receiver. Address data appears on mainframe DISPLAY A.
S2	ENABLE B double action pushbutton switch	When depressed, assigns the module as an address (register) signaling receiver. Address data appears on mainframe DISPLAY B.
S3	ENABLE SUPV double action pushbutton switch	When depressed, assigns the module as an SF line signaling receiver. Line signaling on input ports L1 and L2 appears on the LED supervision indicators.
S4	PROGRAM momentary action pushbutton switch	When depressed, places the module in the program mode. Programmable parameters may be reviewed and changed via the mainframe KEYPAD. The PRGM indicator lights to show that a parameter differs from its initial pre-programmed value. Exit from program mode occurs via the mainframe KEYPAD.
DS1	PRGM light emitting diode	Lights to indicate that one or more of the programmable parameters has been changed and differs from its initial pre-programmed value.
DS2	EN light emitting diode	Lights to show the module is enabled i.e., one or more of the ENABLE A, ENABLE B, or ENABLE SUPV switches are depressed.
DS3	L2 light emitting diode	Lights during the presence of voice band energy on input port L2.
DS4	L1 light emitting diode	Lights during the presence of voice band energy on input port L1.

Notes:

1. When a 2760-17 module is enabled as an address-only receiver (ENABLE SUPV switch released), the module detects only address signaling present on port L1. Signaling present on port L2 is ignored i.e., use of port L2 is not required. If only ENABLE A or only ENABLE B of the 2760-17 module is depressed, another module may usually be assigned to also process address signaling. However, if ENABLE A and ENABLE B of the 2760-17 module are both depressed, no other module may be assigned as an address receiver.

2. When both ENABLE A and ENABLE B are depressed, address signaling appears only on DISPLAY A for all 2760-17 register display modes except mode 3. Both ENABLE A and ENABLE B must be depressed to obtain a complete mode 3 register display.

D. Specifications

3.11 Table C gives the Model 2760-17 SF RECEIVER specifications. Figure 4 shows the specified operating region for the module.

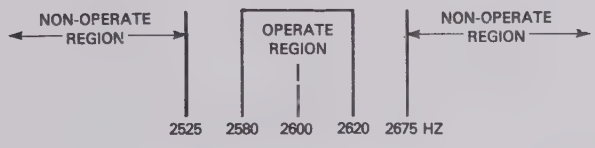
TABLE C

OVERALL SPECIFICATIONS

RECEIVE

Frequency Detection

Operate region



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Detection accuracy ±1 Hz

Level Detection

Operate region

B02641-01

Detection accuracy ±2 dB

TABLE C (Cont)

Pulse Width Detection

Notes:

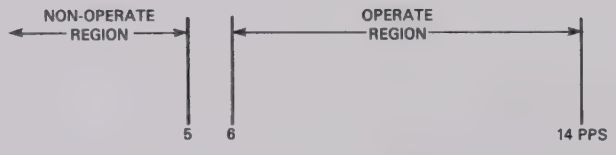
1. Pulse width (tone-on period) measurements for address (register) signaling detection are not displayed. Pulse width measurements are used to determine speed and percent break, which are displayed in units of pps and % break.
2. Pulse width measurements for supervision (line) signaling detection include event-to-event, tone-on, and tone-off periods. These defined pulse width measurements are not displayed, but are used to determine supervision events and violations. An exception is the measured period from connect (seizure) to the next event, which is displayed in address display mode 1B (see DISPLAY MODES section of Table A).

Minimum pulse width response	36 msec
Minimum interpulse period	25 msec
Maximum pulse interruption ignored	9 msec after 20 msec of steady state tones
Detection accuracy	±5 msec

ADDRESS (REGISTER) DETECTION

Pulse Speed Detection

Operate region



B02641-02

Detection accuracy	±0.2 pps at 6 pps
	±1 pps at 14 pps

Percent Break Detection

Operate region	See Fig. 1.
Detection accuracy	±3% at 6 pps
	±8% at 14 pps

TABLE C (Cont)

SUPERVISION (LINE) DETECTION	
Note: An initial 500 msec of on-hook (tone-on) in both forward and backward directions is required before detection of supervision signaling can begin.	
Connect (Seizure) Detection	
Connect event	Off-hook (tone-off) period must exceed 50 msec.
Connect detection accuracy	±10 msec
Delay-Dial/Wink-Start Detection	
Delay-dial/wink-start event	Following a line seizure, a delay-dial/wink-start operation must begin within 500 msec.
Delay-dial/wink-start detection accuracy	±10 msec
Answer Detection	
Answer event	The off-hook (tone-off) period of an answer event must be greater than or equal to the programmed determination time for answer.
Answer detection accuracy	±15 msec
Disconnect (Clear-Forward) Detection	
Disconnect event	The on-hook (tone-on) period of a disconnect event must be greater or equal to the programmed determination time for disconnect.
Disconnect detection accuracy	±15 msec
Hangup (Clear-Back) Detection	
Hangup event	The on-hook (tone-on) period of a hangup event must be greater or equal to the programmed determination time for hangup.
Hangup detection accuracy	±15 msec
Idle State Detection	
Idle determination	500 msec of on-hook (tone-on) in both forward and backward directions
Note: The idle determination period normally occurs after the disconnect and hangup time-out periods.	

TABLE C (Cont)

VIOLATION RECOGNITION

Address (Register) Signaling

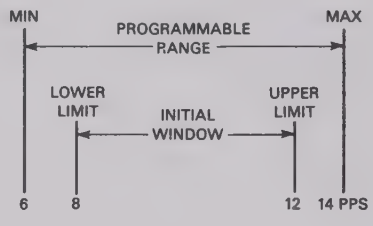
1. pulse speed violation
2. percent break violation
3. pulse level violation

Supervision (Line) Signaling

1. on/off-hook (tone-on/off) time violation
2. on-hook (tone-on) level violation

Programmable Parameters

Pulse speed violation limits



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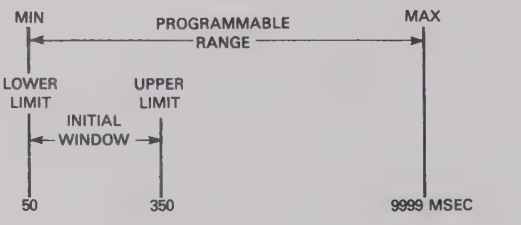
Percent break violation limits

Variable (see Fig. 10)

Connect period violation limits

Note: Connect period is from seizure to the next event (delay-dial, wink-start, or dial pulsing).



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Delay start dial violation limits

Note: Delay start dial refers to the tone-off interval of delay-dial or wink-start. The start-dial signal ends the tone-off period.

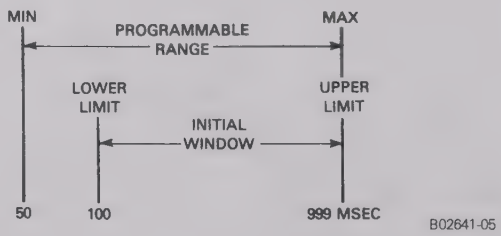

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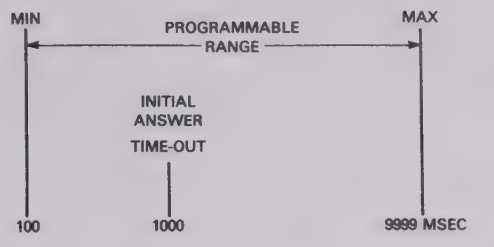
TABLE C (Cont)

Answer determination time-out



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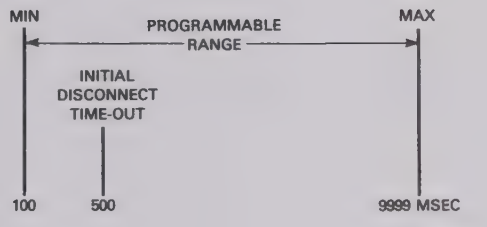
Disconnect determination time-out



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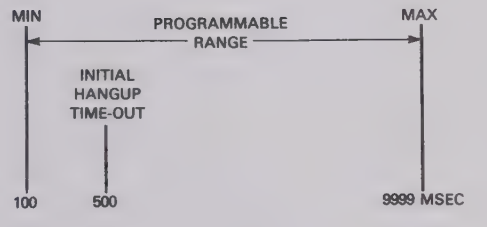
Hangup determination time-out



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Level violation limits

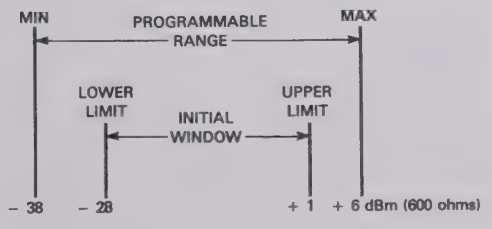

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TABLE C (Cont)

DISPLAY MODES

Address Display

Mode 1A — Displays dialed digits only (no violations shown).

Mode 1B — Displays period from connect (seizure) to next event, dialed digits, and interdigital periods.

Mode 2 — Displays dialed digits and SBLN (speed, percent break, level, and violating pulses of a digit) violation codes.

Mode 3 — Displays average pulse speed and percent break, minimum interdigital period, minimum pulse speed and percent break, and maximum pulse speed and percent break.

Accuracy of displayed parameters

DISPLAYED PARAMETER	MODE 1B DISPLAY
period from connect to next event	The displayed interval has an accuracy of ±5 msec.
interdigital periods	Displayed interdigital values have an accuracy of ±5 msec.

DISPLAYED PARAMETER	MODE 3 DISPLAY
average pulse speed	Displayed speed has an accuracy of ±0.2 pps at 6 pps, and an accuracy of ±1 pps at 14 pps.
average % break	Displayed % break has an accuracy of ±3% at 6 pps, and an accuracy of ±8% at 14 pps.
minimum interdigital period	Displayed period has an accuracy of ±15 msec.
minimum pulse speed	Displayed period has an accuracy of ±0.2 pps at 6 pps, and an accuracy of ±1 pps at 14 pps.
minimum % break	Displayed period has an accuracy of ±3% at 6 pps, and an accuracy of ±8% at 14 pps.
maximum pulse speed	Displayed period has an accuracy of ±0.2 pps at 6 pps, and an accuracy of ±1 pps at 14 pps.
maximum % break	Displayed period has an accuracy of ±3% at 6 pps, and an accuracy of ±8% at 14 pps.

TABLE C (Cont)

Supervision Display	
Mode 1	Displays seized port indicator and supervision event codes.
Mode 2	Displays seized port indicator, supervision event codes, and GPL (gap, pulse, and level) violation codes.
MAINFRAME DISPLAY INTERFACE	seven-segment alphanumeric display
Address Display Codes	
Digits 0 through 9	codes 0 through 9
Digits 11 through 19	codes •1 through •9
SBL (speed, percent break, and level) violation codes	0 = no violation 1 = marginally low 2 = marginally high 3 = excessively high 4 = excessively low
N (violating pulses of a digit) codes	1 = 1st pulse, 2 = 2nd pulse, 3 = 3rd pulse, etc.
Supervision Display Codes	
Seized port indicator	1 = input port L1 2 = input port L2
Supervision event codes	1 = connect 2 = answer 3 = disconnect 4 = hangup 6 = block condition 7 = delay-start dial 5, 8, and 9 not used 0 = idle •1 = glare (double-seizure) condition •2 = short answer (answer period greater than 500 msec but less than programmed answer time-out period) •6 = nonstandard block condition
GPL (gap, pulse width, and level) violation codes	0 = no violation 1 = marginally low 2 = marginally high 3 = excessively high 4 = excessively low

TABLE C (Cont)

LATCH AND RESET	
Latch (hold condition)	Latches on answer and idle
Reset	Resets on connect (seizure) and glare (double seizure)
PHYSICAL CHARACTERISTICS	
Size	7.6 cm (3.0 in) wide (equivalent to two standard single width modules)
Weight	Approximately 1.2 kg (2 lb. 6 oz.)
ENVIRONMENTAL REQUIREMENTS	
Operating temperatures	5°C to 40°C (41°F to 104°F)
Relative humidity	0 to 95%, noncondensing
POWER REQUIREMENTS	Supplied by Model 2760 mainframe

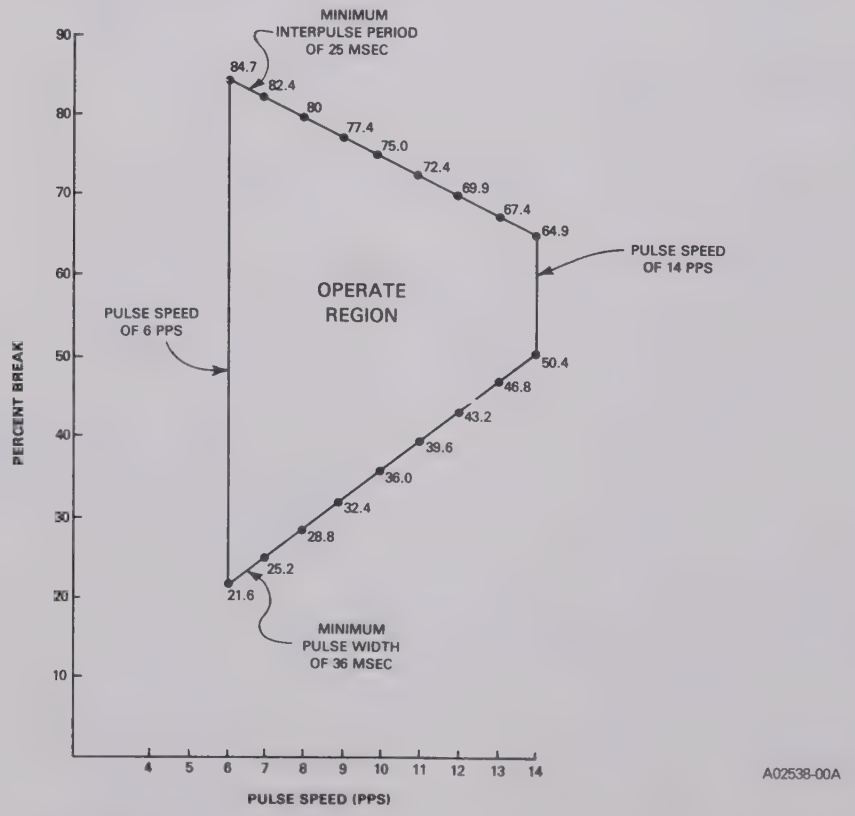


Fig. 4—Percent Break Versus Pulse Speed

4. OPERATION

A. General

4.01 This part describes how to use and operate the Model 2760-17 SF RECEIVER plug-in module. Figure 25 in Part 7 is an overall block diagram of the module.

B. SF Signaling System

4.02 The single frequency, or SF signaling system, was initially developed for long haul toll circuits. It provides for transmitting and receiving both address and supervisory signaling information by means of tone pulses.

4.03 Modern SF signaling systems utilize a frequency of 2600 Hz for signaling in both directions. Because of this, SF signaling may be used only on 4-wire circuits.

4.04 The SF unit converts DC signaling to 2600 Hz tone pulses for transmission over the circuit to the far end. The far end SF unit converts the received tone pulses back into DC signaling. Signaling in the far-to-near direction is accomplished in the same way. The DC signaling may be either E&M or loop.

4.05 In the idle (on-hook) condition a steady SF tone is normally transmitted in both directions at a level of −20 dBm below the voice level (TLP). For signaling a 12 dB pad is removed in the SF unit and the SF tone is transmitted at a level of −8 dBm below the voice level (TLP). This feature provides increased signaling reliability by improving the signal-to-noise ratio.

4.06 Once signaling is completed the tone is removed from the circuit in both directions and conversation may begin. Upon disconnect and hang-up tone is reapplied to the circuit in both directions at a level of −20 dBm below the voice level (TLP).

4.07 SF units are slow and are generally limited to 8 to 12 pulses per second and 56 to 69 percent break. They are used primarily today for supervision signaling on trunks equipped for MF (address) dial pulsing.

C. Verification Tests

4.08 The following tests verify that the plug-in module is in good working order prior to any circuit testing.

4.09 Initial Conditions — Mainframe and Module

4.10 Ensure the following conditions are met before proceeding with the module verification tests.

(a) Instrument is correctly fused and rear panel switch is set for the appropriate voltage (115/230).

Warning: The instrument may be severely damaged if the fuse or switch setting is incorrect.

(b) Instrument is plugged in to an AC electrical power source of the correct voltage (3-wire grounded type outlet).

(c) Ground binding post on rear panel is connected to central office ground bus. Number 14 AWG wire or equivalent is recommended.

(d) The following front panel pushbutton switches are released:

RCL SUPV
NO ERASE
HOLD ERROR
HOLD MATCH
RESET AUTO.

(e) All plug-in module ENABLE switches are released.

(f) Instrument is not connected to any circuits to be tested.

4.11 Power Up

4.12 This test verifies AC power has been correctly applied to the instrument:

STEP	PROCEDURE
1	Depress POWER switch.
	Verification:
	Blower fan runs. LEAD DIGIT IDENT shows 001. L1 OFF HOOK lights. L2 OFF HOOK lights.

4.13 Module Tests

4.14 This test verifies the module is in good working order:

STEP	PROCEDURE
1	Depress ENABLE A switch. Verification: EN indicator lights.
2	Momentarily depress PROGRAM switch. Verification: DISPLAY A shows 00 r dISPLAY 1. DISPLAY B shows L dISPLAY 1.
3	Release ENABLE A switch. Verification: DISPLAY A and B goes blank. EN indicator extinguishes.
4	Repeat steps 1 through 3 for ENABLE B switch.
5	Depress ENABLE SUPV switch. Verification: EN indicator lights.
6	Momentarily depress PROGRAM switch. Verification: DISPLAY A shows 00 r dISPLAY 1. DISPLAY B shows L dISPLAY 1.
7	Release ENABLE SUPV switch. Verification: DISPLAY A and B goes blank. EN indicator extinguishes.

D. Display Assignments

4.15 The 2760-17 module is one of several modules that the mainframe can accept. Usually, an enabled module can perform more than one function. The 2760-17 module can function as an "A" direction receiver, as a "B" direction receiver, or as a supervision (line) signaling receiver. The mainframe permits several functions at one time, but allows only one module to perform a given function. Two modules cannot be enabled to perform the same function at the same time. However, some modules can perform different functions simultaneously.

4.16 "A" direction receiver and "B" direction receiver are general terms which refer to the DISPLAY A or B the signaling is directed towards. Specifically for the 2760-17 module, "A" direction receiver means that the monitored SF address signaling appears on mainframe DISPLAY A. Similarly, "B" direction receiver means that the monitored SF address signaling appears on mainframe DISPLAY B. The 2760-17 module may be enabled to function both as an "A" direction receiver and as a "B" direction receiver for mode 3 operation.

4.17 Depressing the ENABLE A pushbutton enables the 2760-17 module as an "A" direction receiver. SF address signaling appears on mainframe DISPLAY A. Similarly, depressing the ENABLE B pushbutton enables the 2760-17 module as a "B" direction receiver. SF address signaling appears on mainframe DISPLAY B. However, if both ENABLE A and ENABLE B are depressed, the 2760-17 module functions only as an "A" direction receiver, and the SF address signaling only appears on mainframe DISPLAY A, not on DISPLAY B.

4.18 This is true for all address (register) signaling display modes except mode 3. In mode 3, address signaling information appears on both DISPLAY A and B. With both the ENABLE A and B switches depressed, no other module can be enabled as an address signaling receiver.

4.19 Depressing the ENABLE SUPV pushbutton enables the 2760-17 module as a supervision (line) signaling receiver. The supervision signaling appears on the six LED mainframe supervision indicators. If the RCL SUPV switch is depressed the supervision signaling will also appear on DISPLAY A.

4.20 The operator may at any time change the receiver function of the 2760-17 module. If the operator tries, while changing the 2760-17 module assignment, to enable a function conflicting with the assignment of another module, the mainframe PRGM ERROR indicator blinks on and off to alert the operator. The operator must resolve the conflict by locating and disabling the enabled modules so that only the required module is enabled to perform the desired function.

4.21 After successfully enabling the 2760-17 module, another module could subsequently cause an assignment conflict. The EN indicators on some modules blink to flag them as the conflicting module. The operator must resolve the conflict by either disabling the appropriate module or changing the 2760-17 module assignment.

E. Programmable Parameters

4.22 The Model 2760-17 SF RECEIVER has 11 programmable parameters. Programmable means the operator is able to specify and set the value of the parameter within its minimum and maximum limits. This is accomplished by means of the Model 2760 mainframe assembly KEYPAD.

4.23 The 11 programmable parameters are:

No.	Parameter
00	Register Display Mode and Supervision Display Mode
01	Dial Display Mode
02	Pulses Per Second
03	Percent Break
04	Connect
05	Delay Start Dial
06	Answer
07	Disconnect
08	Hang Up
09	L1 Level
10	L2 Level

The 11 parameters are number 00 to 10.

4.24 The first two parameters, 00 and 01, pertain to the display mode selection for both address (register) and supervision (line) signaling. Parameters 02 and 03, pulsing speed and percent break, pertain only to address signaling violations. Parameters 04 and 05 pertain to tone-off interval violations for connect (seizure) and delay dial or wink start operation supervision events. Parameters 06, 07, and 08 provide timing detection criteria for answer, disconnect, and hang up supervision events. Tone level parameters 09 and 10 provide additional violation detection criteria for address signaling tone pulses and for disconnect and hang up supervision events.

4.25 All 11 programmable parameters, A and B DISPLAY appearance, initial values, minimum and maximum programmable values, and descriptions are given in Table D.

TABLE D

MODEL 2760-17 PROGRAMMABLE PARAMETERS

PARAMETER AND INITIAL VALUES	MINIMUM/MAXIMUM PROGRAMMABLE VALUES	DESCRIPTION
A 00 r DISPLAY 1	1,2,3	r = Register display 1 = Mode 1-mode 1A or 1B depending on parameter 01 DIAL DISP 2 = Mode 2-address digits and parameter violations 3 = Mode 3-average pulse speed and percent break, minimum pulse speed and percent break, maximum pulse speed and percent break, minimum interdigital period
L DISPLAY 1 B	1,2	L = Supervision display 1 = Mode 1-seized port and supervisory signals 2 = Mode 2-seized port, supervisory signals, and parameter violations
A 01 DIAL DISP 1	1,2	Determines mode 1 display of parameter 00 r DISPLAY 1 1 = Mode 1A-address digits only 2 = Mode 1B-period from connect (seizure) to first event and address digits with interdigital periods ***Note:*** The initial value of dial display may either be 1 or 2 as set by internal switch S5-1. Refer to paragraphs 2.04 through 2.09.

TABLE D (Cont)

PARAMETER AND INITIAL VALUES	MINIMUM/MAXIMUM PROGRAMMABLE VALUES	DESCRIPTION
A 02 080 120 PPS (10) B	60-140 pps	Pulses per second times 10 on DISPLAY A
A 03 560 690 BREAK (10) B	Variable (Refer to paragraphs 4.26 - 4.31)	Percent break times 10 on DISPLAY A
A 04 0050 0350 CONNECT B	50-9999 msec	Interval between connect (seizure) and next event (delay-dial, wink-start, or dial outpulsing)
A 05 100 999 DELAY START DIAL B	50-999 msec	Tone-off interval of delay-dial or wink-start operation, which is ended by a start-dial signal ***Notes:*** 1. For delay-dial, initial lower and upper limits are 100 and 999 msec as shown. 2. For wink-start, initial lower and upper limits are 100 and 350 msec (refer to paragraphs 2.04 -2.09)
A 06 1000 ANS B	100-9999 msec	Answer determination time-out
A 07 0500 DISCONNECT B	100-9999 msec	Disconnect (clear forward) determination time-out
A 08 0500 HANGUP B	100-9999 msec	Hangup (clear back) determination time-out
A 09 −28 01 L1 LEVEL B	−38 to +6 dBm	Signal level at input port L1
A 10 −28 01 L2 LEVEL B	−38 to +6 dBm	Signal level at input port L2

4.26 Mode 1A or 1B Selection

4.27 Parameter 01 Dial Display enables the operator to select between a choice of two options for parameter 00 Register Display, mode 1. The two options are mode 1A and mode 1B.

4.28 In mode 1A only the received address digits are displayed. In mode 1B the interval between connect (seizure) and the next event, the address digits, and the interdigital periods (IDP) are all displayed.

4.29 The initial selection of mode 1A or 1B is made at the time of module installation by means of internal switch S5-1. Refer to paragraphs 2.04 through 2.09. After installation the operator may select mode 1A or 1B by means of the mainframe KEYPAD.

4.30 Pulses Per Second and Percent Break Selection

4.31 Parameter 02 Pulses per Second allows the operator to specify and set the desired value of the parameter for the test conditions expected to be encountered. Parameter 03 Percent Break minimum and maximum limits are uniquely determined by the pulse speed limits selected and the break and make constraints.

4.32 SF dial pulsing consists of a series of tone-on and tone-off intervals. Terms associated with dial pulsing are shown in Fig. 5. As shown, a dial pulse has three interrelated parameters (pulse width, pulse speed, and percent break). The values of pulse width and pulse speed determine the value of percent break.

4.33 In the 2760-17 module, system requirements place restrictions on permissible break (tone-on) and make (tone-off) intervals. These constraints are:

(a) A minimum of 36 msec for break. At least 36 msec of continuous tone-on is required for acceptance of a tone as a valid pulse signal.

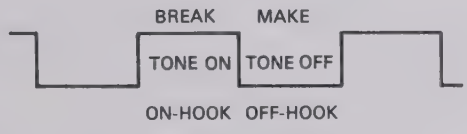
(b) A minimum of 25 msec for make. After detection of a valid pulse signal, a tone-off interval of less than 25 msec is ignored.

(c) A maximum of 180 msec for make. The 2760-17 considers a tone-off interval of more than 180 msec to be an interdigital period.

4.34 Figure 6 shows the relationship between pulsing speed and percent break. Two vertical pulse speed plots (one at 6 pps and another at 14 pps) and two percent break plots (one with a make period equal to 25 msec and another with a pulse width period equal to 36 msec) are shown. Note that these four plots enclose the operate region previously defined by Fig. 4. For measurements in this region, the value of disconnect parameter 08 must be greater than 175 msec.

4.35 Programmable parameter 02 allows the operator to select pulsing speed violation limits between a minimum of 6 pps and a maximum of 14 pps. Selected pulse speed limits together with break and make constraints determine minimum and maximum violation limits allowed for percent break (programmable parameter 03). Pulse speed violation limits are initially set at 8 pps (lower limit) and 12 pps (upper limit), and as a result, minimum and maximum programmable limits for percent break are respectively 44 and 70%. These initial programmable percent break limits are bounded by the solid line rectangle shown in Fig. 6. Initially, the percent break limits are set at 56% (lower limit) and 69% (upper limit), which are indicated by the broken lines within the solid rectangle shown by Fig. 6.

4.36 Each time a lower or upper limit for pulse speed is changed, the 2760-17 module calculates new minimum and maximum limits for percent break. New programmable limits may differ from the previous programmable limits. Therefore, if a previously programmed lower or upper limit for percent break falls outside a respective new minimum or maximum limit, the 2760-17 module automatically sets parameter 03 to the newly calculated minimum or maximum limit.



$$\text{PULSE WIDTH} = \text{BREAK}$$

$$\text{PULSING SPEED} = \frac{1}{\text{BREAK} + \text{MAKE}}$$

$$\text{PERCENT BREAK} = \frac{\text{BREAK}}{\text{BREAK} + \text{MAKE}} \times 100$$

THUS: Percent Break = (Pulse Width)x(Pulsing Speed)x100

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Fig. 5—SF Dial Pulsing Terms

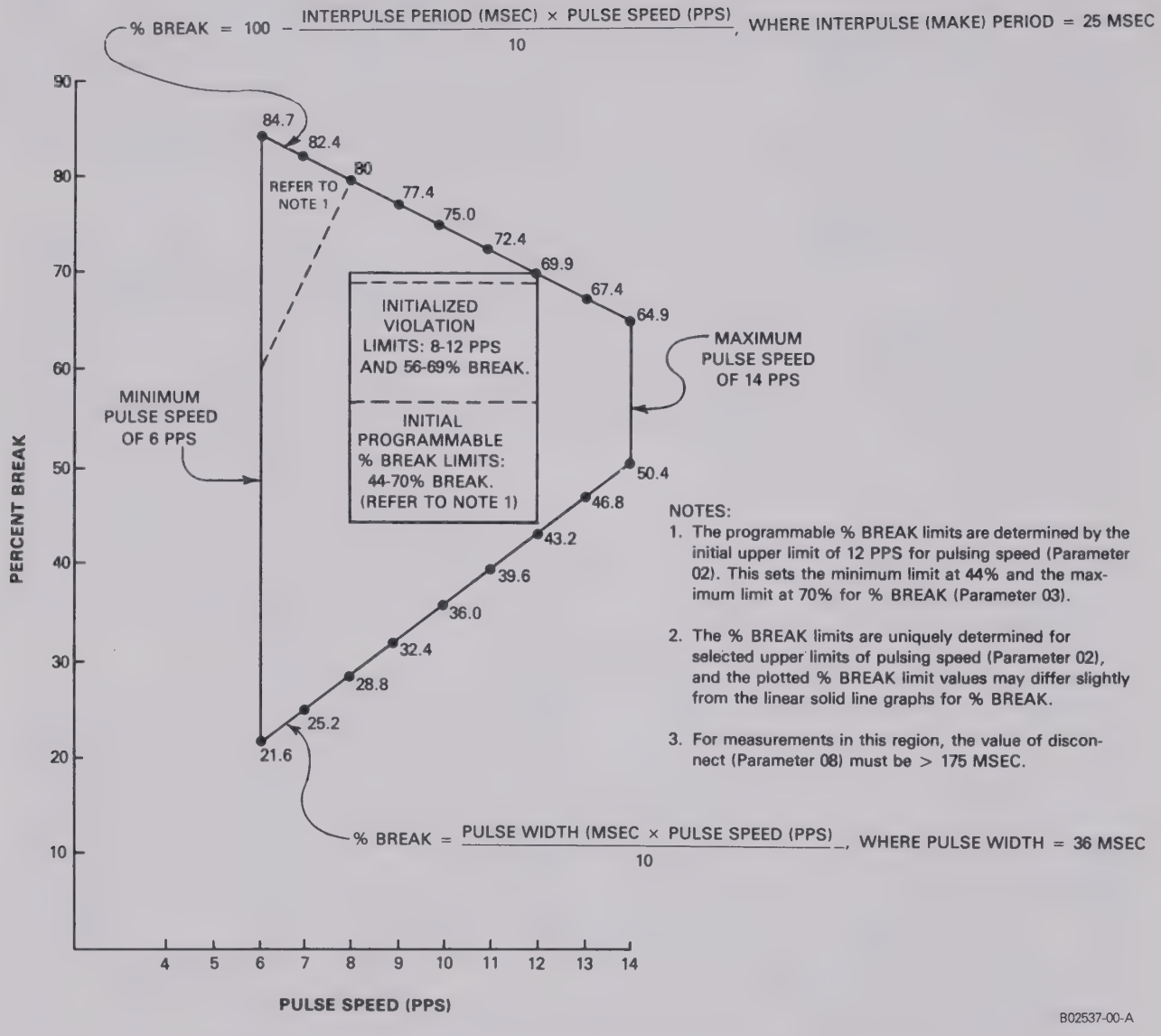
% BREAK = 100 − INTERPULSE PERIOD (MSEC) × PULSE SPEED (PPS) / 10, WHERE INTERPULSE (MAKE) PERIOD = 25 MSEC
PERCENT BREAK
PULSE SPEED (PPS)
84.7
82.4
80
77.4
75.0
72.4
69.9
67.4
64.9
50.4
46.8
43.2
39.6
36.0
32.4
28.8
25.2
21.6
REFER TO NOTE 1
INITIALIZED VIOLATION LIMITS: 8-12 PPS AND 56-69% BREAK.
INITIAL PROGRAMMABLE % BREAK LIMITS: 44-70% BREAK. (REFER TO NOTE 1)
MAXIMUM PULSE SPEED OF 14 PPS
MINIMUM PULSE SPEED OF 6 PPS
% BREAK = PULSE WIDTH (MSEC × PULSE SPEED (PPS) / 10, WHERE PULSE WIDTH = 36 MSEC
NOTES:
1. The programmable % BREAK limits are determined by the initial upper limit of 12 PPS for pulsing speed (Parameter 02). This sets the minimum limit at 44% and the maximum limit at 70% for % BREAK (Parameter 03).
2. The % BREAK limits are uniquely determined for selected upper limits of pulsing speed (Parameter 02), and the plotted % BREAK limit values may differ slightly from the linear solid line graphs for % BREAK.
3. For measurements in this region, the value of disconnect (Parameter 08) must be > 175 MSEC.
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Fig. 6—Programmable Limits of Pulse Speed and Percent Break

4.37 Controlled Outpulsing Selection

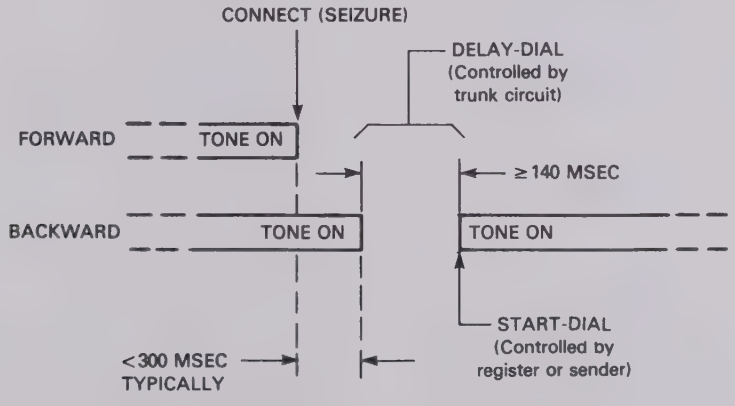
4.38 Parameters 04 and 05 are tone-off intervals associated with delay-dial and wink-start circuit operation. Specifically, parameter 04 is the tone-off interval between connect (seizure) and the next event, i.e. delay-dial, wink-start, or dial outpulsing. Parameter 05 is the tone-off interval of the delay-dial or wink-start operation which is ended by a start-dial (tone-on) signal.

4.39 Delay-dial and wink-start operations are two methods of controlled outpulsing.

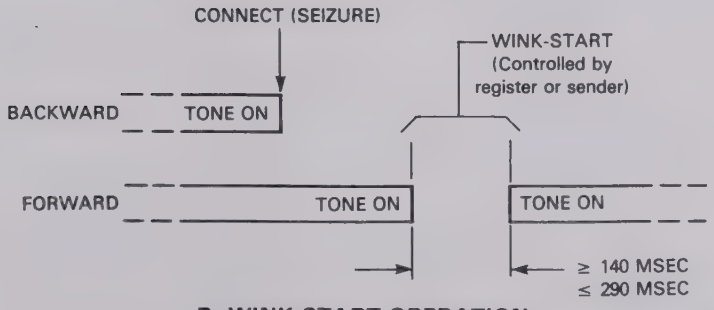
4.40 Internal switch S5-2 enables the 2760-17 module to monitor the two types of controlled outpulsing circuits. Switch S5-2 is set during installation for the type of circuit operation expected. Refer to paragraphs 2.04 through 2.09. For controlled outpulsing circuits, the calling office cannot begin outpulsing (dial pulsing) until it receives an appropriate signal from the called office. Delay-dial and wink-start operation are the two types of controlled outpulsing used. Dial outpulsing usually begins 70 msec after receipt of a start-dial signal or wink-start operation. Figure 7 illustrates the major characteristics of the delay-dial and wink-start operations.

4.41 To be correctly interpreted by the 2760-17 module, a delay-dial or wink-start operation must begin within 500 msec following connect (seizure). A delay-dial or wink-start operation which begins after this 500 msec determination period will be misinterpreted as an answer-hangup event sequence. In addition to this detection requirement, programmable parameter 05 DELAY START DIAL provides a programmable violation criterion for the tone-off interval of either a delay-dial or wink-start operation.

4.42 For noncontrolled outpulsing circuits, dial outpulsing can begin almost immediately after connect (seizure). Normally the calling office waits 150 to 210 msec to allow operation of the far end circuits. The exact amount of the delay depends on the type of office. Usually, SF signaling is not used with immediate-dial circuits.



A. DELAY-DIAL OPERATION



B. WINK-START OPERATION

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Fig. 7—Controlled Outpulsing

4.43 Answer, Disconnect, and Hang Up Selection

4.44 Parameter 06 Answer determines the tone-off interval which is interpreted as an answer supervision event. The initial value is set at 1000 msec.

4.45 Parameter 07 Disconnect (calling party) determines the tone-on interval which is interpreted as a disconnect supervision event. The initial value is set at 500 msec.

4.46 Parameter 08 Hang Up (called party) determines the tone-on interval which is interpreted as a hang up supervision event. The initial value is set at 500 msec.

4.47 The minimum and maximum programmable values for parameters 06, 07, and 08 are from 100 to 9999 msec.

4.48 Receive Level Selection

4.49 Parameters 09 and 10 specify the expected range of signal level at input ports L1 and L2 respectively. Thus, one level parameter may be set for the transmitted level, and the other level parameter set for the received level. The circuit to be monitored must be connected to the mainframe in a manner consistent with the selected level parameters. The transmit pair must be connected to the input port expecting transmit levels, and the receive pair must be connected to the input port expecting receive levels.

4.50 The window limits of both L1 and L2 level parameters 09 and 10 are adjustable in unit (1 dB) steps from a high of +6 dB down to a low of −30 dB. Below −30 dB the next lower adjustment is −32 dB, followed by −35 dB, and −38 dB. Therefore, a lower limit input value of −31 dB results in a lower limit setting of −32 dB, an input value between −33 dB and −35 dB results in a −35 dB limit, and an input value between −36 dB and −38 dB results in a −38 dB limit.

F. Non-Programmable Parameters

4.51 Besides the programmable parameters, several parameters cannot be reviewed or changed.

4.52 When first enabled or either manually or remotely reset, the 2760-17 module requires 500 msec of on-hook (tone-on) in both forward and backward directions before it can begin monitoring supervision signaling, or before it can monitor address signaling if the module is assigned both supervision and address receiver functions. However, if the module is assigned only the address receiver function (ENABLE SUPV switch released), the module begins monitoring address signals on input port L1 immediately once the module is enabled or reset. Address signals on input port L2 are ignored.

4.53 When in the idle state, an off-hook (tone-off) period exceeding 50 msec is considered to be a connect (seizure) supervision event. Signaling on the seized input port is called forward signaling, and signaling on the other port is called backward signaling.

4.54 At the start of a connect (seizure) event a 500 msec period ensues to determine the presence of a delay-dial or wink-start operation. To be correctly detected by the 2760-17, a delay-dial or wink-start event must begin before the end of this 500 msec period.

4.55 An interdigital period (tone-off in the forward direction) has a minimum value of 180 msec for display modes 1 and 2, and a minimum value of 370 msec for display mode 3.

4.56 Following the programmed disconnect (clear forward), or hangup (clear backward) determination time-out, a minimum 500 msec on-hook (tone-on) period in both forward and backward directions is considered to be an idle condition.

G. Programming

4.57 Initial Values

4.58 The Model 2760-17 SF RECEIVER module is preprogrammed at the factory with an initial value for each of the 11 parameters. The preprogrammed values are typical, average, or normal values.

4.59 When it is desired to change the initial preprogrammed value for any parameter, the operator may do so by means of the mainframe KEYPAD. The new value entered via the KEYPAD overrides the initial preprogrammed value.

4.60 To remind the operator that one or more of the 11 initial preprogrammed parameter values have been changed, the module PRGM indicator lights. When the instrument is turned off the module always reverts to the initial preprogrammed parameter values. Keying in C99 will also restore all parameters to their initial values.

4.61 Changing Parameter Values

4.62 To review or change parameters, the operator momentarily presses the module PROGRAM pushbutton. The parameters appear on mainframe DISPLAY A and DISPLAY B. The mainframe KEYPAD is used to change the displayed parameter. An underscore (_) functions as a prompting character to show how many digits remain to be entered in the parameter undergoing editing. Table E lists the functions of the keypad keys during reviewing and editing of the programmable parameters. Figure 8 outlines a general approach to review and edit parameters.

4.63 As a parameter value changes, the module checks the validity of the change with respect to:

- Minimum and maximum range values
- Lower limit less than upper limit
- Completeness of input. If the input is invalid prompting characters replace the incorrect input.

4.64 The sequence shown in Fig. 9 to change receive level parameter 10 from −28 01 to −38 06 is a typical programming sequence.

4.65 The following procedure may be used to change the value of any of the 11 parameters:

STEP	PROCEDURE
1	Depress ENABLE A or B switch. ***Note:*** If any other module is assigned to that display you will not be able to enable the module. The mainframe PRGM ERR indicator will also flash on and off.
2	Momentarily depress the PROGRAM switch. Display will show: 00 r dISPLAY 1. L dISPLAY 1.
3	Key in 1, 2, or 3 to change the display mode.
4	Key in D. Display will show: 01 dIAL dISP 1.
5	Key in 1 or 2 to change the display mode (1 = mode 1A and 2 = mode 1B)
6	Key in D. Display will show: 02 080 120 PPS (10).
7	To change the first three digits (080) key in 060 to 139. To change the second three digits (120) key in 061 to 140. This is the number of PPS multiplied by 10. ***Note:*** The first three digits must be the lower value.
8	Key in D. Display will show: 03 560 690 brEAK (10).
9.	To change the first three digits (560) key in 440 to 699. To change the second three digits (690) key in 441 to 700. This is the percent break value multiplied by 10. ***Note:*** The first three digits must be the lower value. Also refer to paragraph 4.35.
10	Key in D. Display will show: 04 0050 0350 CONNEct.
11	To change the first four digits (0050) key in 0050 to 9998. To change the second four digits (0350) key in 0051 to 9999. ***Note:*** The first four digits must be the lower value.
12	Key in D. Display will show: 05 100 999 dELAY StArt dIAL.
13	To change the first three digits (100) key in 050 to 998. To change the second three digits (999) key in 051 to 999. ***Note:*** The first three digits must be the lower value.
14	Key in D. Display will show: 06 1000 AnS.
15	To change the initial value key in 0100 to 9999.
16	Key in D. Display will show: 07 0500 diSconnEct.

STEP	PROCEDURE
17	To change the initial value key in 0100 to 9999.
18	Key in D. Display will show: 08 0500 HAnGUP.
19	To change the initial value key in 0100 to 9999.
20	Key in D. Display will show: 09 −28 01 L1 LEUEL.
21	To change the first two digits (−28) key in the desired numerical value. To program a + reading key in an * and then the desired numerical value. Values of +05 to −38 may be programmed in the first position. Values of +06 to −35 may be programmed in the second position. ***Note:*** The first position must be the lowest value.
22	Key in D. Display will show: 10 −28 01 L2 LEUEL.
23	To change values repeat step 31.
24	To restore all parameters to their initial values key in C,9,9.
25	To exit the program mode key in #.

TABLE E

KEYPAD COMMANDS TO REVIEW AND EDIT PROGRAMMABLE PARAMETERS

KEY	DESCRIPTION
0—9	To edit parameters To call a parameter with C To select the display mode
A	A is equivalent to zero—can be used instead of the 0 key.
B	To display minimum/maximum values, initial values, and current values of a parameter. Command B triggers the following sequence on the mainframe display; 1. Minimum and maximum range values displayed for 2 seconds 2. Initial values displayed for 2 seconds 3. Current values returned to the display 4. Control returned to the keypad.
C	To jump to parameter XY—where $00 \leq XY \leq 10$. Command C followed by two digits accesses the parameter specified by the two digits. If an invalid parameter number is specified, the display defaults to parameter 00. If the two digits equal 99 then the module restores all parameters to their initial values.
D	To call the next parameter: Command D changes the display to the next higher parameter. If a next higher parameter does not exist, the display defaults to parameter 00.
*	Assigns a + sign to a positive value of level (> 0 dBm). Level values not preceded by an * are assumed to be negative (< 0 dBm). The display shows negative values with a minus (−) sign and positive values without a sign.
#	Command # exits the program mode. Exit is not allowed if any parameter is incomplete.

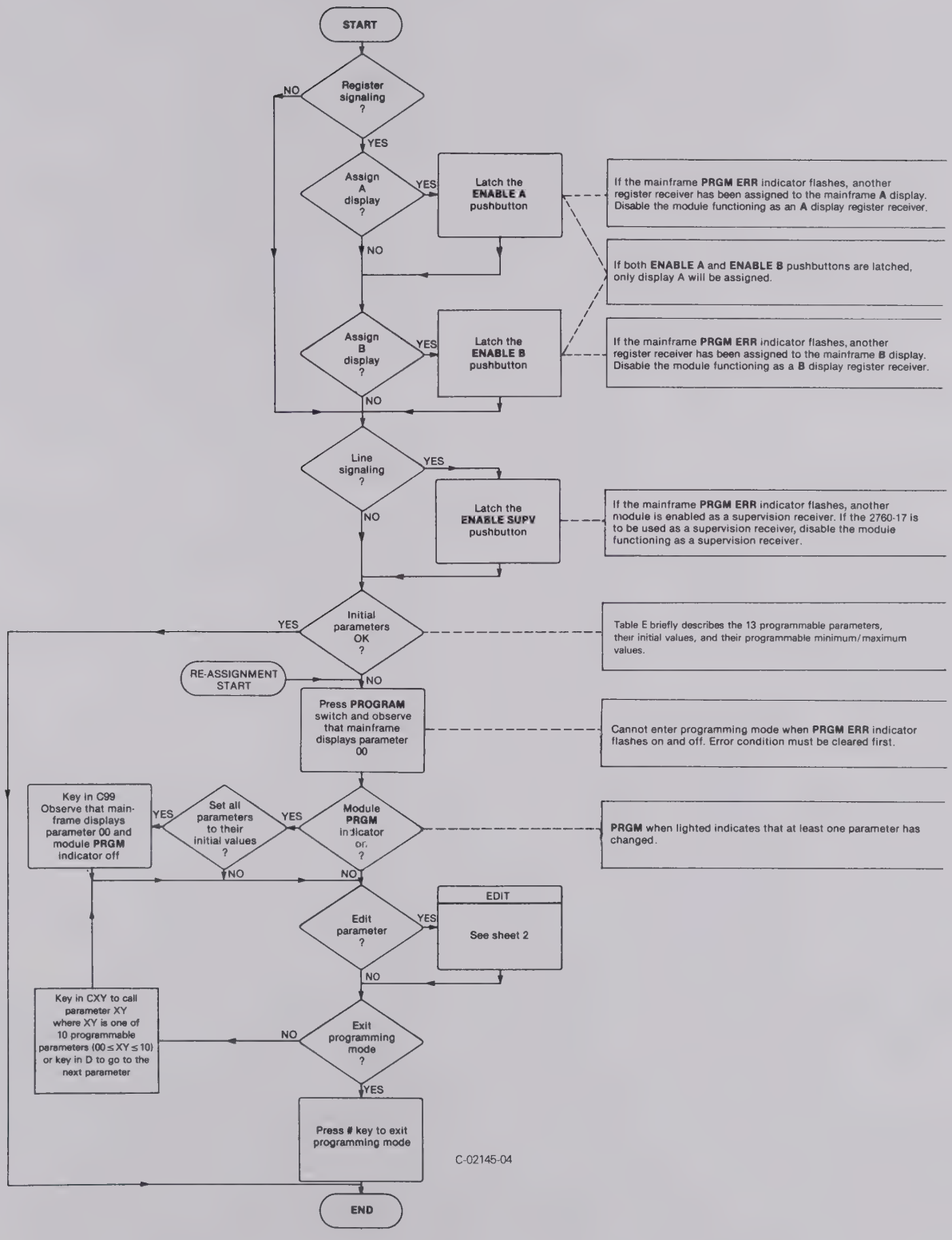

START
Register signaling ?
NO
YES
Assign A display ?
YES
Latch the ENABLE A pushbutton
If the mainframe PRGM ERR indicator flashes, another register receiver has been assigned to the mainframe A display. Disable the module functioning as an A display register receiver.
NO
If both ENABLE A and ENABLE B pushbuttons are latched, only display A will be assigned.
Assign B display ?
YES
Latch the ENABLE B pushbutton
If the mainframe PRGM ERR indicator flashes, another register receiver has been assigned to the mainframe B display. Disable the module functioning as a B display register receiver.
NO
Line signaling ?
YES
Latch the ENABLE SUPV pushbutton
If the mainframe PRGM ERR indicator flashes, another module is enabled as a supervision receiver. If the 2760-17 is to be used as a supervision receiver, disable the module functioning as a supervision receiver.
NO
Initial parameters OK ?
YES
Table E briefly describes the 13 programmable parameters, their initial values, and their programmable minimum/maximum values.
RE-ASSIGNMENT START
NO
Press PROGRAM switch and observe that mainframe displays parameter 00
Cannot enter programming mode when PRGM ERR indicator flashes on and off. Error condition must be cleared first.
Key in C99 Observe that mainframe displays parameter 00 and module PRGM indicator off
YES
Set all parameters to their initial values ?
YES
Module PRGM indicator on ?
PRGM when lighted indicates that at least one parameter has changed.
NO
NO
EDIT
Edit parameter ?
YES
See sheet 2
NO
Key in CXY to call parameter XY where XY is one of 10 programmable parameters (00 ≤ XY ≤ 10) or key in D to go to the next parameter
NO
Exit programming mode ?
YES
Press # key to exit programming mode
C-02145-04
END

Fig. 8—Programming Flowchart (Sheet 1 of 2)

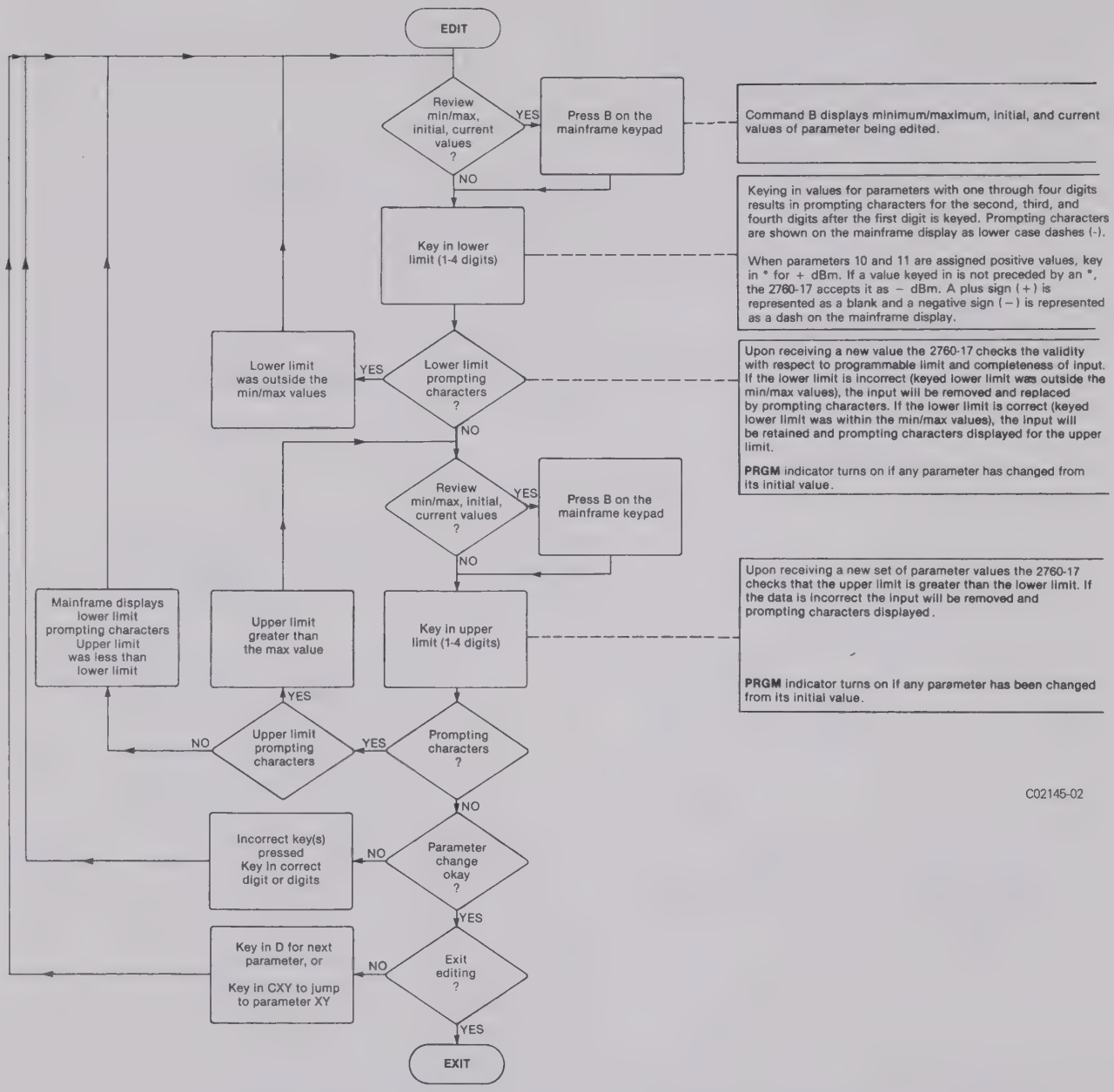

EDIT
Review min/max, initial, current values ?
YES
Press B on the mainframe keypad
Command B displays minimum/maximum, initial, and current values of parameter being edited.
NO
Key in lower limit (1-4 digits)
Keying in values for parameters with one through four digits results in prompting characters for the second, third, and fourth digits after the first digit is keyed. Prompting characters are shown on the mainframe display as lower case dashes (-).
When parameters 10 and 11 are assigned positive values, key in * for + dBm. If a value keyed in is not preceded by an *, the 2760-17 accepts it as − dBm. A plus sign (+) is represented as a blank and a negative sign (−) is represented as a dash on the mainframe display.
Lower limit was outside the min/max values
YES
Lower limit prompting characters ?
Upon receiving a new value the 2760-17 checks the validity with respect to programmable limit and completeness of input. If the lower limit is incorrect (keyed lower limit was outside the min/max values), the input will be removed and replaced by prompting characters. If the lower limit is correct (keyed lower limit was within the min/max values), the input will be retained and prompting characters displayed for the upper limit.
PRGM indicator turns on if any parameter has changed from its initial value.
NO
Review min/max, initial, current values ?
YES
Press B on the mainframe keypad
NO
Mainframe displays lower limit prompting characters Upper limit was less than lower limit
Upper limit greater than the max value
Key in upper limit (1-4 digits)
Upon receiving a new set of parameter values the 2760-17 checks that the upper limit is greater than the lower limit. If the data is incorrect the input will be removed and prompting characters displayed.
PRGM indicator turns on if any parameter has been changed from its initial value.
YES
NO
Upper limit prompting characters
YES
Prompting characters ?
C02145-02
NO
Incorrect key(s) pressed Key in correct digit or digits
NO
Parameter change okay ?
YES
Key in D for next parameter, or
Key in CXY to jump to parameter XY
NO
Exit editing ?
YES
EXIT

Fig. 8—Programming Flowchart (Sheet 2 of 2)

Press PROGRAM pushbutton

Display shows parameter 00.

Key in C09

Parameter 10 appears as:

0	9		–	2	8			0	1					
							L	1		L	E	V	E	L

Key in 38*6 . . . an error, should have keyed 38*06

Parameter 10 appears as:

0	9		–	3	8			6	_					
							L	1		L	E	V	E	L

Key in 0 . . . the resulting upper limit value of 60 exceeds the maximum range value for this parameter - prompting characters replace the keyed upper limit value.

Parameter 10 appears as:

0	9		–	3	8		_	_	_					
							L	1		L	E	V	E	L

Key in *060 . . . extra zero entered, display overflows

Parameter 10 appears as:

0	9		–	0	_									
							L	1		L	E	V	E	L

Key in D, C, or # . . . no change, input rejected

Parameter 10 appears as:

0	9		–	0	_									
							L	1		L	E	V	E	L

Key in 000 . . . the resulting equal lower and upper limits are not permissible - prompting characters replace the keyed lower limit input.

Parameter 10 appears as:

0	9		_	_	_		–	0	0					
							L	1		L	E	V	E	L

Key in 38*06 (correct entry)

Parameter 10 appears as:

0	9		–	3	8			0	6					
							L	1		L	E	V	E	L

Key in B

1. minimum/maximum range values shown for 2 seconds

Parameter 10 appears as:

0	9		–	3	8			0	6					
							L	1		L	E	V	E	L

2. initial values shown for 2 seconds

Parameter 10 appears as:

0	9		–	2	8			0	1					
							L	1		L	E	V	E	L

3. current values re-appear

Parameter 10 appears as:

0	9		–	3	8			0	6					
							L	1		L	E	V	E	L

B02502-00

Note: Other parameters may be reviewed or changed. To exit the program mode, press the # key.

Fig. 9—Typical Parameter Programming Sequence

H. Display Interpretation

4.66 The decoded signaling appears on the appropriate mainframe display. Address (register) signaling goes either to DISPLAY A or B as selected by the ENABLE A and ENABLE B pushbutton switches. The address (register) signaling is also stored in the A and B DISPLAY memories. A memory (one for each display) can store up to 240 characters including blank spaces while the display can only show up to 16 characters at a time. If a display shows updated information as the address (register) signaling is being monitored, the display is a real-time display. If the displayed information is previously stored data, then the display is referred to as a recall display.

4.67 Recall is entered when one of the mainframe's scroll/cursor (left or right) switches is depressed. As soon as a scroll/cursor switch is depressed, the 2760 enters a hard latch state and ignores all subsequent address (register) signaling until manually or remotely reset. The following indicators identify the recall mode:

- Mainframe LATCH indicator lighted
- One vertical pair of digit/codes on the mainframe's dual display blinks.

4.68 The blinking is called the CURSOR. The mainframe's LEAD DIGIT IDENT read-out identifies the CURSOR's position within the stored sequence of digits/codes.

4.69 The CURSOR may be moved by depressing either of the scroll/cursor switches. When the CURSOR reaches either end of the mainframe's dual display, additional stored signals are scrolled back into the display. Thus all of the stored register signaling information can be recalled from the data memories and reviewed on the display. The recalled digits/codes appear on the display in the exact sequence that they were originally received.

4.70 The manual mainframe reset via the RESET MAN switch or a remote reset applied at the RESET REM port returns the 2760 to normal operation.

4.71 The supervision (line) signaling information from the module (ENABLE SUPV switch depressed) is shown in real time on the six mainframe LED supervision indicators. Only the last supervision event is shown. The line signaling is also stored in a supervision memory. The contents of the supervision memory may be shown on the mainframe DISPLAY A in real time or recalled by depressing the SUPV RCL pushbutton switch. The supervision memory stores only 16 characters; therefore the supervision data may not be scrolled like the address (register) signaling data.

4.72 Register Display

4.73 The 2760-17 provides several register display modes to show monitored address signaling data:

(a) In mode 1A the display shows dialed digits only. See Fig. 10.

(b) In mode 1B the display shows dialed digits and interdigital periods. The first value displayed enclosed in brackets is the period from connect (seizure) to the next event, followed by dialed digits and interdigital periods also enclosed in brackets. See Fig. 11.

(c) In mode 2 the display shows dialed digits together with violation codes and violating pulses of digits which failed to meet programmed limits. Violation codes and violating pulses are enclosed in brackets immediately following a displayed digit. See Fig. 12.

(d) In mode 3 the display shows average, minimum, and maximum values for pulsing speed and percent break. The minimum interdigital period (IDP) is also displayed. See Fig. 13.

(e) Additional submodes are accessible while in mode 3. These submodes provide displays of stored digit data.

4.74 Either mainframe display A or display B (but not both) is used to show signaling data in display modes 1A, 1B, and 2. However, both displays A and B are used to show address signaling data in mode 3. Therefore, the 2760-17 module must be enabled as both an A-direction and B-direction receiver to obtain a complete mode 3 data display.

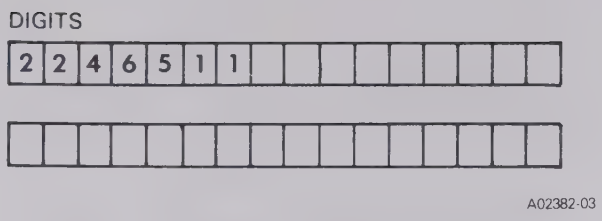


Fig. 10—Mode 1A Register Display

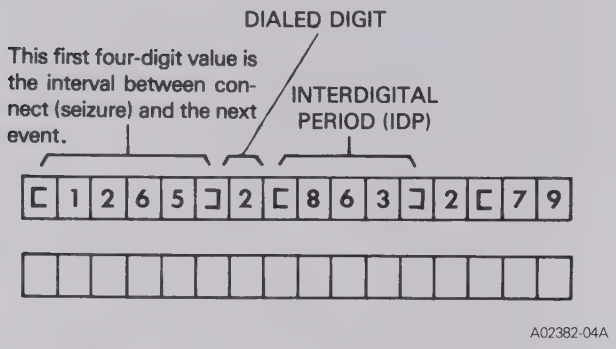

DIALED DIGIT
This first four-digit value is the interval between connect (seizure) and the next event.
INTERDIGITAL PERIOD (IDP)
A02382-04A

Fig. 11—Mode 1B Register Display

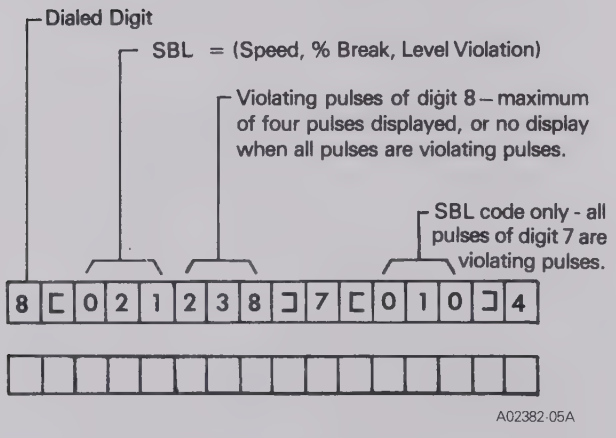

Dialed Digit
SBL = (Speed, % Break, Level Violation)
Violating pulses of digit 8 – maximum of four pulses displayed, or no display when all pulses are violating pulses.
SBL code only - all pulses of digit 7 are violating pulses.
A02382-05A

Fig. 12—Mode 2 Register Display

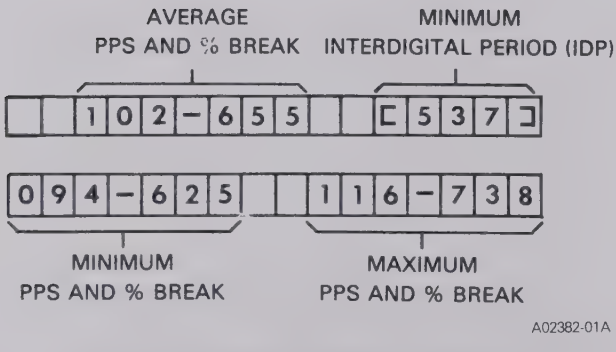


Fig. 13—Mode 3 Register Display

4.75 Mode 1A/1B Address Signaling Display

4.76 A dialed digit consists of a series of short 2600 Hz pulses. Ten pulses are used to represent dial digit 0. For dial digits 1 through 9, the number of pulses used equals the numerical value of a dialed digit. An interdigital tone-off period of 180 msec or more separates any two digits.

4.77 When interdigital periods separating two or more dial digits are less than 150 msec, the 2760-17 assumes these periods are make periods of a digit, and the module displays a digit value equal to the total number of pulses used. For example, the 2760-17 displays digit 9 for dialed digits 4 and 5 if these digits are separated by an interdigital period less than 150 msec. For this example, it is assumed that a digit dialed before the 4 or after the 5 was separated by an interdigital period greater or equal to 180 msec. The summing of pulses in this way could exceed a value of ten; therefore, the module displays symbols •1 through •9 for digit pulse sums 11 through 19. Pulse sums greater than 19 are also displayed as •9.

4.78 Figure 10 illustrates a mode 1A address display. As shown, only detected dial digits are shown in mode 1A. When the mainframe NO ERASE push-button switch is depressed, more than a single call sequence may be displayed with a blank space separating each call.

4.79 Figure 11 illustrates a mode 1B display. The first four digit value shown in mode 1B is the interval between connect (seizure) and the next event (delay-dial, wink-start, or dial outpulsing), followed by dialed digits and interdigital periods. The last digit of a call sequence is shown without an interdigital period. Also, the lowest interdigital period shown is 180 msec, and the highest is 999 msec. As in mode 1A, more than one call sequence may be displayed if the mainframe NO ERASE switch is depressed.

4.80 Mode 2 Address Signaling Display

4.81 In mode 2, a "violation" occurs in a digit if one or more pulses fail to meet any of the pulse parameter specifications. The specified parameters are:

(1) Speed — the pulsing rate sets the interval between any two pulses in a digit,

(2) Percent Break — the ratio of break duration to the sum of break (tone-on) and make (tone-off) durations, and

(3) Level — the amplitude of the 2600 Hz tone.

4.82 After completion of a call, a mode 2 dialed digit display might read "0(0101)". The dialed digit precedes the brackets, and the SBLN code is inside the brackets. See Fig. 14 for definitions of the SBL and N violation terms. For the given example, digit 0 had a marginally low percent break (B=1) due to a short first pulse (N=1).

4.83 Because a digit (except digit 1) consists of two or more pulses, conflicting violations could occur from pulse to pulse. Therefore, the SBL code identifies only the first conflicting violation encountered. For example, a digit 0 having a short first pulse followed by a long second pulse would be displayed as "0(01012)". Here, the SBL (with B=1) identifies only the low percent break violation caused by the short first pulse; whereas the N term identifies both the first and second violating pulses. As an added example, display "0(0112345)" again indicates a marginally low percent break violation, as well as a marginally low level violation. The N term identifies the second, third, fourth, and fifth pulses as violating pulses not directly related to the violations defined by the SBL code. Also, for this example, one or more of the remaining pulses (the sixth through tenth pulses) may also have been violating pulses not designated by the N term because N can designate a maximum of four violating pulses. However, when all the pulses of a digit are violating pulses, the N term is not displayed. Only the dialed digit and SBL code (example "0(010)" are shown.

4.84 Mode 3 Address Signaling Display

4.85 Mode 3 address signaling display is different from the previous display modes in that it requires DISPLAY A and B to completely show its information. The need for two displays in mode 3 means that the 2760-17 module must be enabled as both an A direction receiver and a B direction receiver.

4.86 Figure 13 shows the information displayed in mode 3 when the 2760-17 is enabled as an A and B direction receiver. The information consists of (1) the average pulsing speed and percent break of the last digit greater than digit "1", (2) the minimum interdigit period of the call, (3) the minimum pulsing speed and percent break of a call, and (4) the maximum pulsing speed and percent break of the call.

4.87 When a received call ends with one or more digit ones ("2246511" for example), the average pulsing speed and percent break data pertains to the last digit which was not a "1" (digit 5 for the example given). Also, the lowest interdigit period is 350 msec, and the highest period displayed is 999 msec. Finally, when the 2760-17 is enabled in only one direction, the displayed information consists of only the average pulsing speed and percent break together with the minimum interdigit period.

4.88 Although no information on the dialed digits appears in mode 3, the 2760-17 module does retain dialed digit data which may be viewed by use of the left or right scroll/cursor control located on the 2760 mainframe. This stored data consists of information normally shown in a mode 2 address signaling display. Thus, the operator has data available on the digits dialed and on parameter violations that occurred during dialing.

4.89 Operating the display in the recall mode (refer to paragraph 4.67) places the retained data on the dialed digits and parameter violations up on the display. However, the previously displayed mode 3 data is irretrievably lost.

4.90 Alternately, operating the display in the "condensed" mode by keying "*B3" on the mainframe KEYPAD (refer to mainframe manual A2760-00-600) places the dialed digits data without any violation information on the display. In the condensed mode, the display cannot be scrolled and therefore only up to the first 16 dialed digits stored may be displayed.

4.91 Keying "#" to exit the condensed mode returns the mode 2 address signaling display as previously described. The information previously shown in mode 3 cannot be returned to the display.

D[SBLN]

D = dialed digit

S = speed violation code

B = percent break violation code

L = level violation code

N = A one-to-four digit number which identifies specific violating pulses of a dialed digit (N = 134 for example, specifies the first, third, and fourth pulses). A maximum of four pulses are displayed. The N is not displayed when all the pulses of a given dialed digit have violations.

For SBL

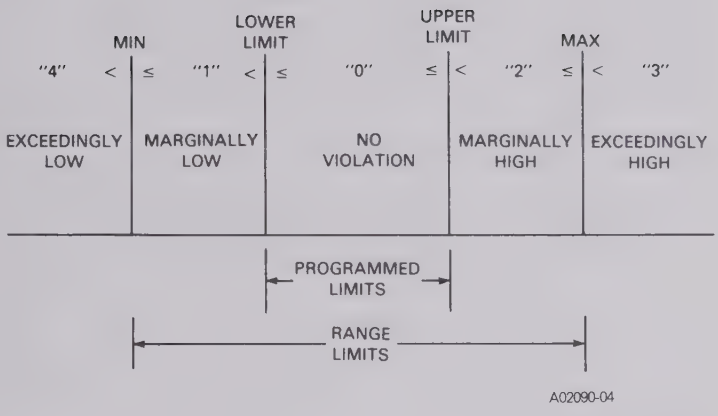
0 = no violation . . .between or equal to the programmed upper and lower limits

1 = marginally low . . . less than the programmed lower limit and greater than or equal to the **min**imum range value

2 = marginally high . . . greater than the programmed upper limit and less than or equal to the **max**imum range value

3 = exceedingly high . . . greater than **max**imum range value

4 = exceedingly low . . . less than the **min**imum range value



NOTE

SIG ERR indicator flashes on and off to alert the operator that the call had a violation.

Fig. 14—Definitions of Address Signaling Violation Terms

4.92 Supervision Display

4.93 The six LED mainframe supervision indicators show the latest supervision event decoded by the 2760-17 module. The accumulated supervision events (line signaling) may be seen on mainframe DISPLAY A by depressing the RCL SUPV pushbutton. Mainframe DISPLAY B shows the system time as long as the RCL SUPV pushbutton remains depressed. Figure 15 illustrates a typical SF signaling sequence. Table F lists the display code and the lighted indicator for each signaling event.

4.94 The supervision display has two modes:

(a) In mode 1 the display shows the supervision events as they occurred, without displaying any violations. See Fig. 16.

(b) In mode 2 the display shows the supervision events and violations if any. See Fig. 17.

4.95 When first enabled or reset, the 2760-17 requires 500 msec of on-hook signaling in both forward and backward directions before it can start monitoring supervision signaling. After this initial 500 msec idle state, an off-hook (tone-off) period exceeding 50 msec is considered to be a connect (seizure) supervision event. The first code shown in mode 1 or 2 identifies the input port on which seizure supervision originated (code 1 for port L1, or code 2 for port L2). Signaling on the seized input port is called forward signaling, and signaling on the other port is called backward signaling (refer to Table F). Following the seized port identification, supervision event codes are shown beginning with connect (code 1).

4.96 The time interval from connect (seizure) to the beginning of the next event (delay-dial, wink-start, or dial outpulsing) is measured by the 2760-17. This measured period is compared to the upper and lower limits of programmable parameter 04 CONNECT. A connect violation occurs when the measured interval falls outside the programmed window limits. In display mode 1, only the detected connect code (without a violation indication) is shown. In display mode 2, the event code as well as a violation indication are shown. Note that there are no gap or level violation indications other than "0" for connect (seizure). See Fig. 18 for definitions of supervision signaling violation terms.

4.97 The next event following connect may be the start of delay-dial, wink-start, or the start of dial pulsing. Following seizure, a 500 msec period ensues to determine the presence of a delay-dial or wink-start operation. To be correctly detected by the 2760-17, a delay-dial (or wink-start) operation must begin before the end of this 500 msec determination period. A delay-dial (or wink-start) operation which begins after the 500 msec period will be misinterpreted as an answer-to-hangup event sequence.

4.98 The off-hook interval of the delay-dial or wink-start operation is also measured. This measured period is compared to the upper and lower limits of programmable parameter 05 DELAY START DIAL. A pulse width violation is designated when the measured interval falls outside the programmed window limits. In display mode 1, only the detected start-dial (on-hook) signal of delay-dial or wink-start operation is shown (code 7 for either operation). In display mode 2, the event code and a violation indication are shown. Note that there are no gap or level violation indications other than "0" for connect (seizure). See Fig. 18 for definitions of violation terms.

4.99 As shown in Fig. 15 dial pulsing normally follows the connect and delay-dial/wink-start events, with answer supervision following dial pulsing. Programmable parameter 06 ANS determines the detection and display of a monitored answer event. For detection of an answer event (code 2), the tone-off state must remain present for the duration of the programmed answer determination time-out period. If the tone-off state of answer remains present for a period greater than 500 msec, but less than the determination time-out period, a short answer event is designated and shown as code •2. When parameter 06 is set to a value less than 500 msec, code •2 is not used; code 2 is then used only if the answer tone-off state remains beyond the programmed determination time. The same answer codes are used for display modes 1 and 2. Note that upper and lower limit violation considerations do not apply to the detection of an answer event, and that answer violation indications are not shown in mode 2.

4.100 Disconnect (clear-forward) and hangup (clear-back) events normally follow an answer event, either one occurring first. To be detected, these events must meet time-out requirements similar to the answer detection requirement. Programmable parameters 07 DISCONNECT and 08 HANGUP determine the detection and display of disconnect and hangup events. The tone-on states of these events must be present for the duration of the programmed determination time-out periods. In addition to the above detection requirements, the tone-on signal level

of these events is measured and compared to the lower and upper limits of programmable parameters 09 L1 LEVEL and 10 L2 LEVEL for a possible signal level violation. Disconnect and hangup event codes (codes 3 and 4) are shown in modes 1 and 2 only when measured tone-on states remain beyond the programmed determination times. In addition to disconnect and hangup event codes in mode 2, violation indications are given when tone-on signal levels fall outside the programmed window limits.

4.101 After a programmed disconnect or hangup determination time-out period, a tone-on state in both forward and backward directions for at least 500 msec is considered an idle condition. Depending on monitored tone-off and tone-on signaling states, blocked conditions may also result. Refer to paragraphs 4.108-4.111 for determination of idle and blocked signaling conditions.

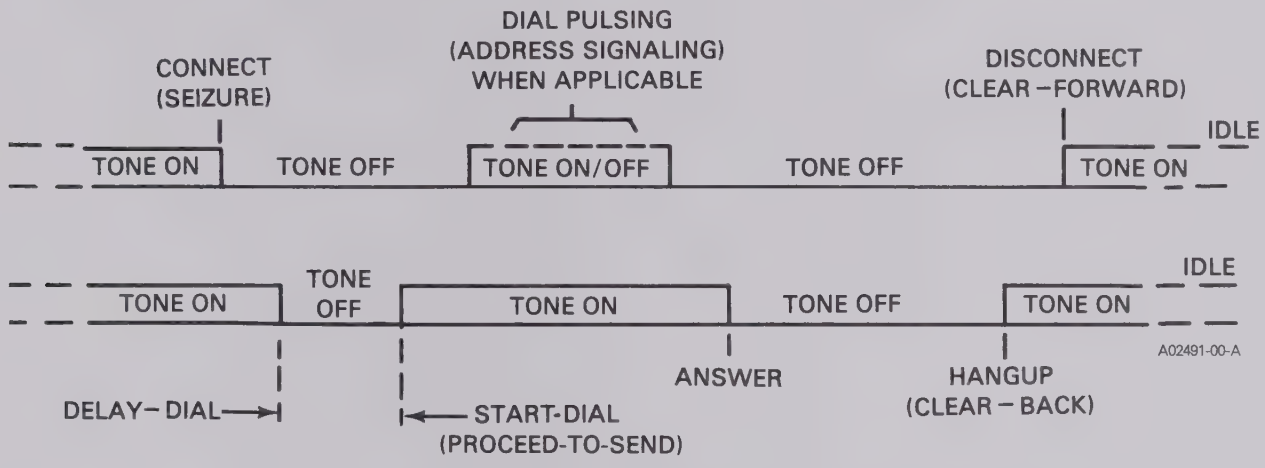


Fig. 15—Typical SF Signaling Sequence

TABLE F

SF SIGNALING DEFINITIONS, INDICATORS, AND CODES

SIGNAL		SF TONE		DISPLAY	
		FORWARD	BACKWARD	INDICATOR	CODE
Idle	on-hook	on	on	none	0
Glare (double seizure)	off-hook	off	off	SEIZURE	•1
Blocking		on	off	BLOCKED	6, or •6 *
		or			
		off	on		
Forward Signals					
Connect (seizure)	off-hook	off	on	SEIZURE	1
Dial pulsing (address)	alternate on-hook and off-hook	on (break) off (make)	on	none	(digit)
Disconnect (clear forward)	on-hook	on	off or on	CLR FWD	3
Backward Signals					
Delay-dial	off-hook	off	off	none	none
Start-dial (proceed-to-send)	on-hook	off	on	none	7
Answer	off-hook	off	off	ANSWER	2, •2 **
Hangup (clear back)	on-hook	off	on	CLR BACK	4

* •6 = Code for nonstandard block

** •2 = Code for short answer period—defined as greater than 500 msec, but less than the programmed determination time for answer. Code •2 is not used when parameter 06 (ANS) is set to a value less than 500 msec.

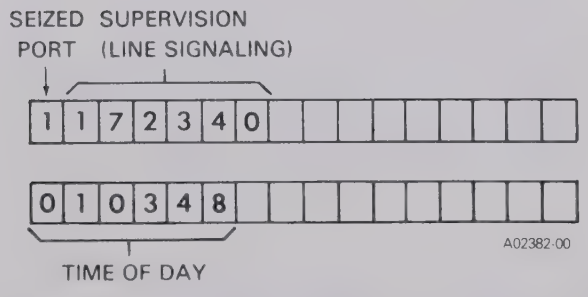


Fig. 16—Mode 1 Supervision Display

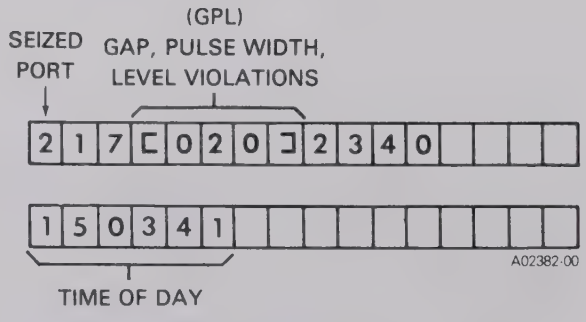


Fig. 17—Mode 2 Supervision Display

C[GPL]

C = supervision event code

G = gap (not used by the 2760-17 as a supervision violation code—it is given a fixed no-violation designation of "0")

P = pulse width (interval between two sequential supervision events)

L = pulse level (tone level of disconnect or hangup event)

For G, P, or L

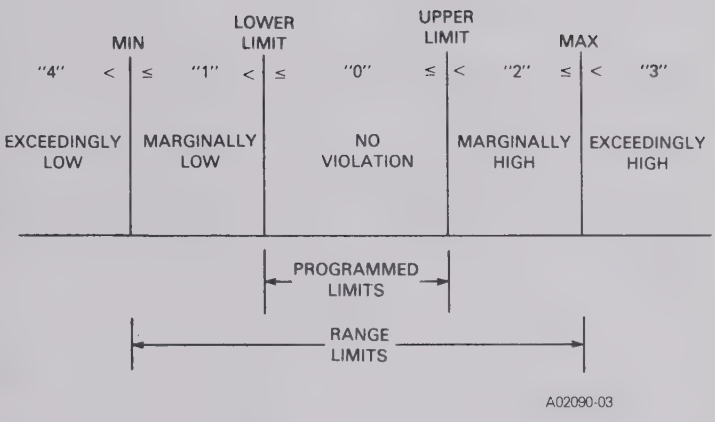
0 = no violation . . . between or equal to the programmed upper and lower limits

1 = marginally low . . . less than the programmed lower limit and greater than or equal to the minimum range value

2 = marginally high . . . greater than the programmed upper limit and less than or equal to the maximum range value

3 = exceedingly high . . . greater than the maximum range value

4 = exceedingly low . . . less than the minimum range value



NOTE

SIG ERR indicator flashes on and off to alert the operator that the call had a violation.

Fig. 18—Definitions of Supervision Signaling Violation Terms

4.102 Mode 1 Supervision Signaling Display

4.103 After completion of a call, a typical supervision display in mode 1 could read: "2172340". The first "2" identifies input port L2 as the port where seizure was detected. The other digits identify the supervision signaling events: 1 = connect (seizure), 7 = start-dial (delay-dial) or wink-start, 2 = answer, 3 = disconnect (clear forward), 4 = hangup (clear back), and 0 = idle.

4.104 Mode 2 Supervision Signaling Display

4.105 In display mode 2, a "violation" occurs if either the pulse width or the level falls outside the programmed limits for a supervision event. After completion of a call, a typical supervision display in mode 2 could read "21(010)723(001)4". The digits outside the brackets refer to supervision events. Supervision events followed by three digits within brackets have one or more violations. The example given indicates a marginally low interval between connect (seizure) and delay-dial/wink-start. It also indicates the received tone level for the DISCONNECT (code 3) was marginally low. See Fig. 18 for definition of violation terms.

4.106 Should the supervision display be unable to store the six characters (digit, two brackets, and three violation codes) required for a violation, the display reverts back to mode 1. If, for example, disconnect (clear forward) had a violation, only code "3" would appear on the display as shown in mode 1. Once the supervision display fills up with 16 characters, no further line signaling is shown on the supervision display; however, the mainframe supervision indicators continue to show the latest signaling event.

4.107 Idle and Blocked Determination

4.108 Figure 19 illustrates the conditions which determine an idle state. A minimum 500 msec on-hook (tone-on) period in both forward and backward directions is required for idle determination. Therefore, the idle determination period normally occurs after both disconnect and hangup events are determined.

4.109 Figure 20 illustrates the various blocked and nonstandard blocked conditions. A forced idle display follows a blocked or nonstandard blocked determination. Note that for a glare double seizure condition (example B) the 2760-17 cannot uniquely determine the forward direction from the backward direction; therefore, the display does not show a seized port identification. Disconnecting both input ports L1 and L2 could appear to the 2760-17 as a glare condition. Also, disconnecting one of the input ports L1 or L2 could appear to the 2760-17 as a blocked condition (example A).

4.110 A blocked state forces an idle determination. The forced idle prevents the 2760-17 from camping on a blocked circuit when operating with a circuit concentrator such as the Model 2776 Trunk Access Unit.

4.111 After power up, enabling of the 2760-17 module, manual or remote reset, or a forced idle state, a 500 msec period of continuous tone-on (on-hook) in both directions is required before the 2760-17 can process SF signaling. This insures that monitoring begins with connect (the start of a call), not in the middle of a call.

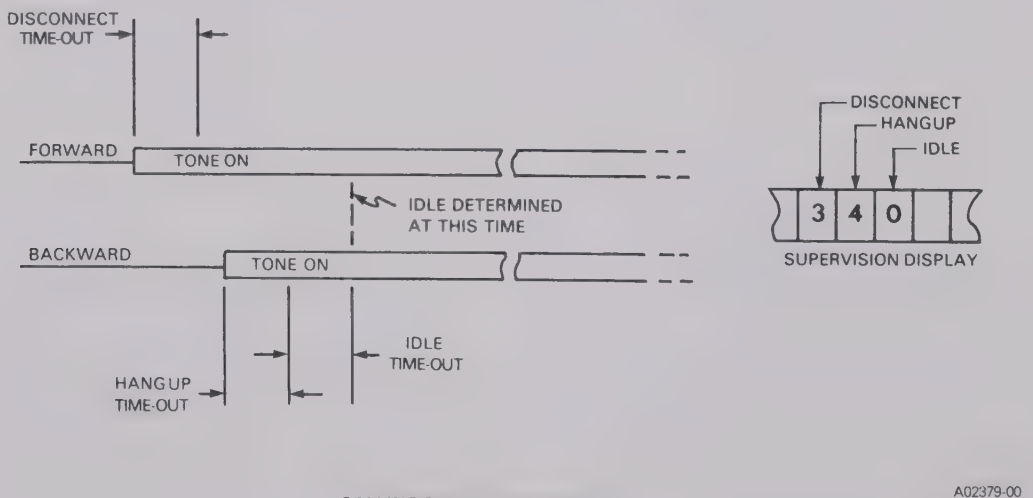
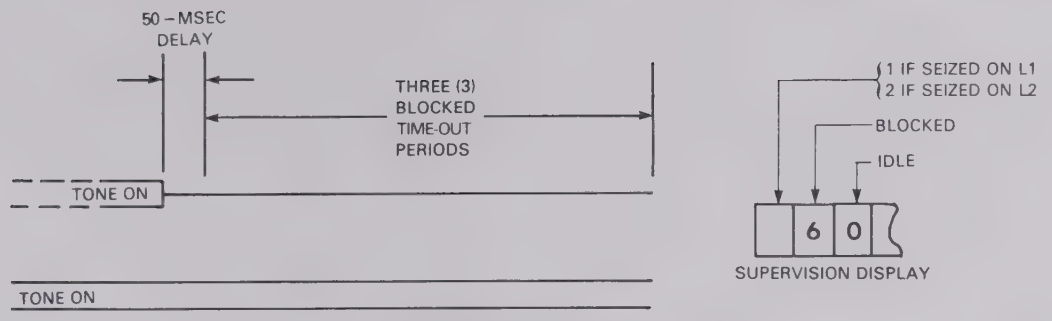
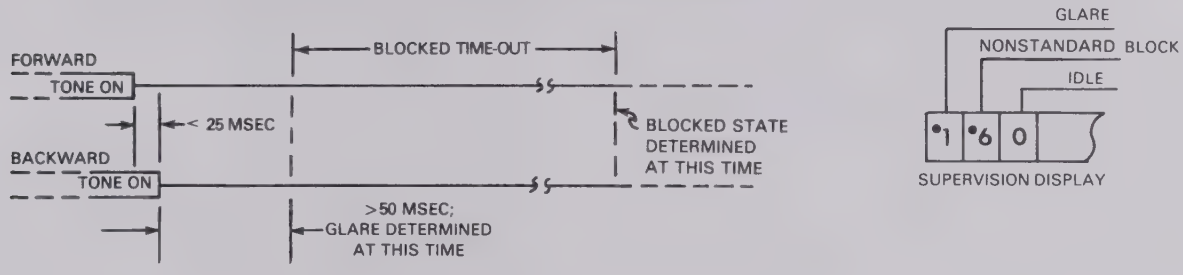


Fig. 19—Idle State Determination

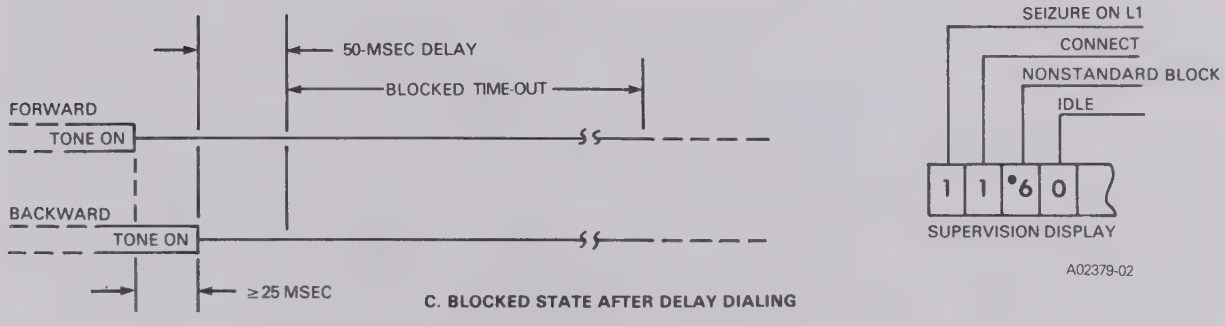


A. BLOCKED STATE AFTER SEIZURE AND BEFORE DELAY DIALING OR ANSWER

A02379-04

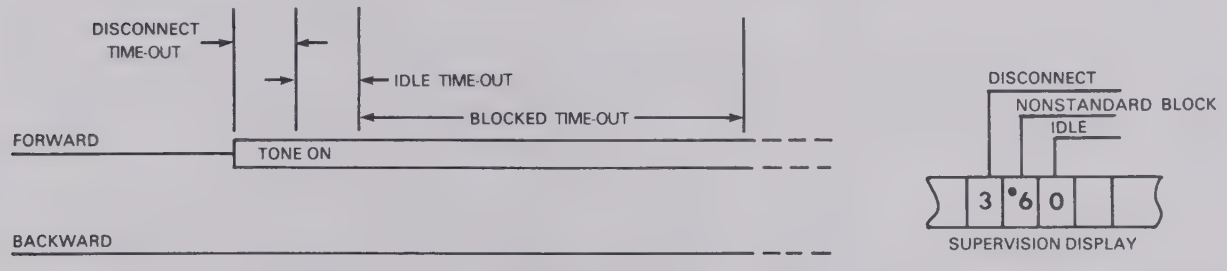


B. BLOCKED STATE AFTER GLARE

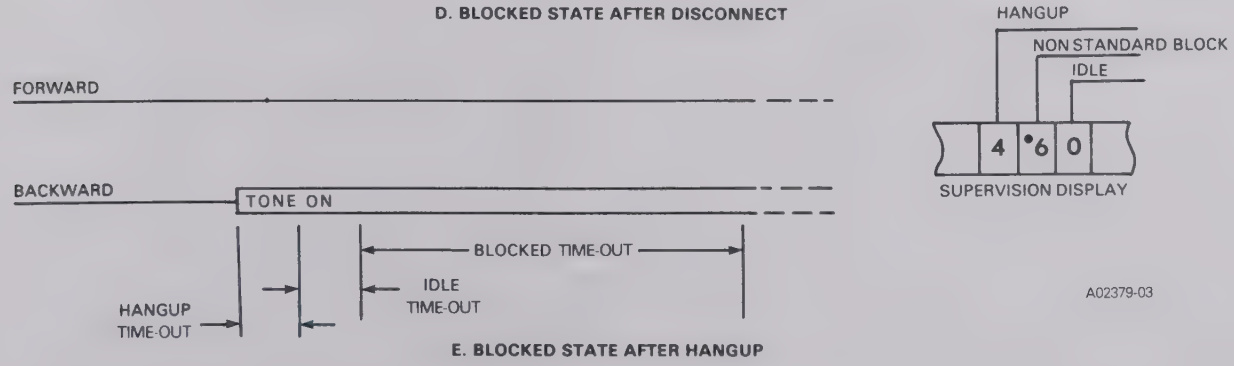


C. BLOCKED STATE AFTER DELAY DIALING

A02379-02



D. BLOCKED STATE AFTER DISCONNECT



E. BLOCKED STATE AFTER HANGUP

A02379-03

Fig. 20—Blocked State Determination

I. Latches and Resets

4.112 Refer to the mainframe manual (A2760-00-600) for definitions and descriptions of latches and resets. The 2760-17 module requests that the 2760 enter into a soft latch state when answer supervision is detected, or when the module determines that an idle condition exists. In a soft latch state, the 2760-17 module cannot accept further address signals.

4.113 If the latch state remains soft, the 2760-17 module may subsequently clear the soft latch state with a reset. A connect (seizure) or a double seizure (glare) supervision causes the generation of a reset signal. The 2760-17 module cannot clear a hard latch. A manual or remote reset is required to clear a hard latch state.

J. Sequence Comparison

4.114 Register signaling codes are stored in data memory and shown on the mainframe until the 2760 enters a soft latch state.

4.115 During the first soft latch state, up to 16 register signaling digits from the DISPLAY A memory are copied into an edit memory. In mode 1 the register display may have blank spaces. If the register display is in mode 2, the data memory may contain violation codes. These blank spaces and violation codes must be deleted prior to copying data into the edit memory. The deletion (or edit) process removes all filler characters (blank spaces), brackets, and all characters between the brackets (violation codes).

4.116 Refer to the Model 2760 operation manual (A2760-00-600) for a description of sequence comparison and programming instructions.

4.117 After the editing and copying process ends, the content of the edit memory is compared with each file of the sequence comparison memory or with the memory for DISPLAY B to determine if the received number (or portion of the number) matches or does not match one of the programmed sequence comparison numbers. Should a sequence match be found or not found as specified, then the soft latch changes into a hard latch if the mainframe HOLD MATCH switch is depressed. If the NO ERASE and the RESET AUTO switches are depressed, sequence comparison occurs only on the first call received.

K. Test Connections

4.118 The 2760 mainframe may be set up in a permanent installation or as a stand-alone portable test set. For permanent installation refer to Part 2 of the mainframe manual (A2760-00-600). Figure 21 shows a typical front panel connection to monitor a four-wire circuit. If the rear terminal barrier strips are used for connections, the connections must be bridging connections since the 2760 acts as a high impedance passive device.

4.119 When instructed to monitor supervision signaling, the 2760-17 must connect (via input ports L1 and L2) with both pairs of the four-wire signaling system to correctly interpret and display SF supervision signaling.

4.120 When instructed to monitor address signaling only, the 2760-17 must connect via input port L1 to the selected pair of the four-wire system to be monitored. Connection of input port L2 to the four-wire system is not required.

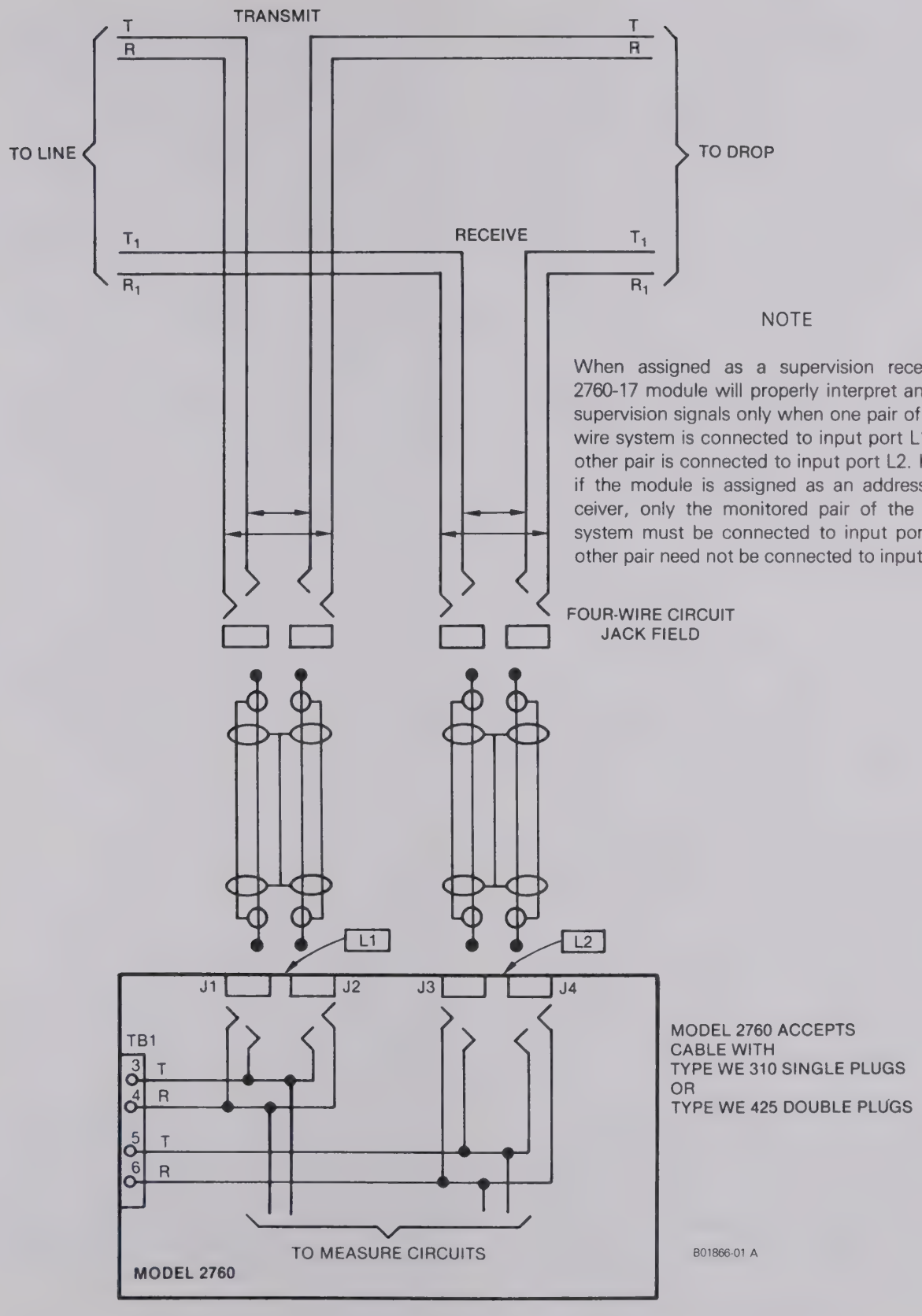


Fig. 21—Typical Front Panel Connections to Monitor Four-Wire Circuits

5. THEORY OF OPERATION

A. General

5.01 This part presents the theory of operation for the 2760-17 SF Receiver. Circuit descriptions are limited to the block and functional levels depicted by Figures 25 and 26 in Part 7. Sufficient reference designators are included in the block and functional diagrams so that the circuit descriptions can be applied to detailed circuit schematics also presented in Part 7 of this manual.

B. Module Operation

5.02 The 2760-17 module uses a single frequency of 2600 Hz to detect and decode both register and line signaling. In general, the module must obtain the following information from a signal appearing on either the L1 or L2 mainframe input port:

- Presence or absence of 2600-Hz energy
- Input signal level
- Relative strength of the 2600-Hz component with respect to the input signal level.

5.03 The SF Receiver monitors register and line signaling consisting of 2600-Hz tone bursts. Both input ports L1 and L2 of the mainframe resident module accept in-band voice energy from a four-wire signaling system under test.

5.04 The 2760-17 conditions the received tone bursts to allow decoding, interpretation, and measurement. The results are stored and displayed by the 2760.

5.05 As shown in Fig. 25 in Part 7, the 2760-17 module consists of the following circuit cards:

- Single Frequency Input A3 (D2760-17-012)
- Digital Interrupt and Interface A1 (D2760-18-018)
- Memory and Timer A2 (D2760-11-019).

5.06 The Single Frequency Input circuit card performs the following functions:

(1) Accepts telecommunication signals . . . single frequency tone bursts . . . on two input lines referred to as L1 (Line 1) and L2 (Line 2).

(2) Shapes the spectrum of L1 and L2 . . . shaping is accomplished with prefilter (audio bandpass filter) and notch (band reject) filter circuits. Filter circuit outputs together with a mainframe-supplied 10-kHz square wave are applied to a hard limiter tone detection circuit.

(3) Produces TTL logic pulses for detected 2600-Hz tone bursts. . . . independent frequency detection pulse generating channels are provided for input ports L1 and L2.

(4) Produces dc voltages L1L and L2L respectively proportional to the rms input voltages of L1 and L2.

5.07 Also, the Single Frequency Input circuit card rejects tones (produces a TTL logic low at the appropriate TDN output) for the following input conditions:

- Signal level at the L1/L2 input is less than −45 dBm
- Signal frequency is below 2525 Hz or above 2675 Hz.

5.08 The Digital Interrupt and Interface circuit card analyzes the information received from Single Frequency Input A3. The circuit card contains manual controls and circuits to provide the following functions:

- Tone change detection
- Level measurement
- Interrupt
- Module enabling
- Module reset
- Module active
- Programming modes
- Decoding functions.

5.09 The Memory and Timer circuit card has ROM and RAM memory to store programming and data specific to the operation of the 2760-17 module. A triple timer, operating under program control, assists the module in monitoring and analyzing the supervision signals. A memory control logic circuit provides the necessary signals for operation of the memory and timer circuit card.

C. Circuit Card Operation

5.10 Single Frequency Input A3

5.11 The single frequency input circuit provides a processed tone output for each audio signal received from the L1 or L2 mainframe input port. As shown in Fig. 26 in Part 7, the single frequency input circuit card has two identical signal processing circuits. Because both circuits operate the same, only one signal processing circuit is discussed in detail.

5.12 The outputs of the input circuit card consist of:

- TD0 (TD1) . . . a positive TTL logic signal with a pulse width that follows the duration of a valid 2600-Hz tone burst
- L1L (L2L) . . . a dc signal with an amplitude proportional to the input signal amplitude at L1 (L2).

5.13 The input signal processing circuit consists of a:

- Prefilter and buffer
- Notch filter and voltage follower
- Hard limiter and inverter
- Narrow bandpass filter
- Full-wave rectifier and envelope detector
- Threshold detector and driver
- Rms-dc converter.

5.14 Prefilter and Buffer

5.15 The prefilter, a bandpass filter consisting of a high-pass filter cascaded with a low-pass filter, passes all frequencies between 720 to 4500 Hz. The buffer applies the filter signal to the hard limiter, 2600-Hz notch filter, and the rms-dc converter. The overall gain of the prefilter and buffer is 7 dB.

5.16 Notch Filter and Voltage Follower

5.17 Received 2600-Hz tones are compared against a dc reference level determined by the output of the notch filter and voltage follower circuit. The notch filter removes the 2600-Hz tone component from the output spectrum of the prefilter.

5.18 The notch filter consists of a generalized-immittance converter circuit configured as a bandstop filter network with a center frequency of 2600-Hz. The voltage follower isolates the notch filter's output, which is a copy of the prefilter's output except that the 2600-Hz component is removed.

5.19 Hard Limiter and Inverter

5.20 In addition to the prefiltered L1 (L2) signal input, the hard limiter circuit receives two other signal inputs; (1) the output of the notch filter and voltage follower circuit, and (2) a 10-kHz square wave signal from the 2760 mainframe. The input from the notch filter determines the dc reference level at the non-inverting input of the hard limiter. The 10-kHz square wave and the prefiltered signal inputs appear at the inverting input of the hard limiter. The hard limiter compares these three input signals and outputs a constant level square wave, the frequency of which is determined by the most significant of the three input signals.

5.21 The output frequencies of the hard limiter are determined by the following input conditions:

(1) With a no-signal at L1 (L2), the 10-kHz dither input captures the hard limiter and a 10-kHz square wave output results. The dither input sets a low amplitude discrimination threshold which prevents unnecessary interrupt requests from the module to the mainframe.

(2) With a −38 dBm or greater signal level present at L1 (L2), the frequency of the limiter's output is determined by comparing the 2600-Hz component level against the limiter's dc reference level.

Note: Switch S1, located at the inverting input of the hard limiter, is factory set in the OFF position. Switch S1 must remain in the OFF position to ensure proper operation of Single Frequency Input A3.

5.22 Narrow Bandpass Filter

5.23 The narrow bandpass filter consists of a generalized-immittance converter circuit configured as a bandpass network with a 2600-Hz center frequency and an 86-Hz bandwidth. The narrow bandpass filter receives the frequency output of the hard limiter and allows a valid tone burst of 2575 to 2625 Hz to pass on to the full-wave rectifier and envelope detector circuit.

5.24 Full-wave Rectifier and Envelope Detector

5.25 The full-wave rectifier and envelope detector circuit receives the 2600-Hz tone output of the narrow bandpass filter and produces a waveform which follows the amplitude of the input tone . . . usually a tone burst of variable duration.

5.26 The rectifier section of the circuit first inverts and half-wave rectifies the input signal, then combines the rectified portion with the original signal. The detector section is a two-stage amplifier network with gain ratios such that the positive output signal is always equal to the absolute value of the tone signal input.

5.27 Threshold Detector and Driver

5.28 The positive output signal of the envelope detector is applied to the threshold detector which uses a hysteresis transfer function to produce a negative TTL signal. The negative signal is inverted by the driver to provide the TD0 (TD1) digital signal to the Digital Interrupt and Interface circuit card. A positive TD0 (TD1) level signals the presence of valid 2600-Hz energy at L1 (L2), and a low level TD0 (TD1) signals the absence of valid 2600-Hz energy.

5.29 RMS-DC Converter

5.30 In addition to the tone detection function, the single frequency input circuit must also provide the digital interrupt and interface circuit card with a dc level input L1L (L2L) proportional to the rms signal level present at L1 (L2). The rms-dc converter receives the prefiltered L1 (L2) signal and generates the required L1L (L2L) dc level. A level input at L1 (L2) of 0.7746 vrms results in an L1L (L2L) level of 1.778 $\pm$ 0.63 Vdc.

5.31 Digital Interrupt and Interrupt A1

5.32 The Digital Interrupt and Interface circuit card analyzes the level and tone data processed by Single Frequency Input A3. The digital interrupt and interface circuit provides the interface control which passes digital data to, and receives data from, the 2760 mainframe. The following functional sections (see Fig. 25 in Part 7) comprise the digital interrupt and interface:

- Module enable and reset control
- Interrupt control
- Module control logic
- Tone change detector and interface control no. 1
- Level measure and interface control no. 2.

5.33 Initiation of enable and reset operation is effected by pushbutton switches ENABLE A (S1), ENABLE B (S2), and ENABLE SUPV (S3). The state of these control switches determines the module assignment . . . as an "A" direction, "B" direction, or supervision receiver.

5.34 The various circuits of the digital interrupt and interface which receive commands from and pass information to the mainframe are treated by the processor as if they are memory locations. This technique of considering input/output circuits as memory locations is called a "memory mapped I/O". The interrupt control circuit generates interrupt requests which are serviced by the processor on a low-to-high number priority basis. All I/O addressing and read/write activity are decoded and controlled by the module control logic.

5.35 Processed tone signals from Single Frequency Input A3 are applied as TTL logic inputs (only TD0 and TD1 are used by the SF Receiver) to tone change detector and interface control no. 1. The level measure circuit monitors dc line signals L1L and L2L, and routes the resulting data to interface control no. 2. Data transfer between the mainframe and interface controls is governed by the processor's use of module programs stored in memory circuits of Memory and Timer A2.

5.36 Before tone and level data can be analyzed and interfaced, the following module and mainframe actions must occur:

- Module must be assigned a function . . . be enabled
- Processor must be reset and the module initialized
- Processor must determine that an assignment does not conflict . . . two modules do not have the same assignment
- Interrupt must be sent to the processor
- Module control logic must be activated.

5.37 When a module is connected to the mainframe but not enabled, the module is partially powered . . . only some of its logic circuits are powered. Communication between the processor and the module cannot occur, and the module is effectively shut down. Enabling the module switches power to the remaining circuits.

5.38 When enabled, the module monitors signals present at the input ports, and generates interrupts as changes of the input signals are detected. Also, the processor can enable or inhibit the interrupt control circuit, can access the function memory stored in the memory and timer circuit card, and can activate the module.

5.39 Full control of the module is available to the processor only when the module is activated. The processor can then use program routines stored in the memory and timer circuit card, and can access memory mapped I/O circuits. Note that more than one module can be enabled but only one module can be activated during the same time. Therefore, after a module is activated, it must be deactivated by the processor before the processor can obtain access to a different module.

5.40 Module Enable and Reset Control

5.41 Latching one of the front panel control switches (ENABLE A, ENABLE B, ENABLE SUPV) determines the module assignment and effects the following signal outputs:

- $\overline{\text{RESIN}}$ signal from the reset generator to the mainframe
- $\overline{\text{RCVA}}$, $\overline{\text{RCVB}}$, or $\overline{\text{SUPV}}$ assignment to the mainframe
- $\overline{\text{AEN}}$, $\overline{\text{BEN}}$, or $\overline{\text{SUPVEN}}$ status signal to Memory and Timer A2
- AEN, BEN, or SUPVEN enabling signal to the interrupt control and interface control no. 2.

5.42 The $\overline{\text{RESIN}}$ signal causes the processor to begin a mainframe and module initialization routine. The processor immediately returns a $\overline{\text{RESOUT}}$ signal to clear the interrupt control and interface controls.

5.43 The mainframe uses the $\overline{\text{RCVA}}$, $\overline{\text{RCVB}}$, or $\overline{\text{SUPV}}$ signal in determining if there is an assignment conflict with another module presently enabled. The $\overline{\text{AEN}}$, $\overline{\text{BEN}}$, or $\overline{\text{SUPVEN}}$ status signals let the processor access the programs of the functional memory located on the memory and timer circuit card. These signals also permit the memory and timer to produce a $\overline{\text{MOD SET}}$ signal. The module control logic uses the $\overline{\text{MOD SET}}$ signal to activate I/O decoding in the digital interrupt and interface circuit card. The control logic also activates the module memory located on the memory and timer circuit card.

5.44 The AEN, BEN, and SUPVEN status signals allow the interrupt control to generate an interrupt . . . $\overline{\text{INT2}}$, $\overline{\text{INT3}}$, and $\overline{\text{INT4}}$ respectively. The AEN, BEN, and SUPVEN signals applied to interface control no. 2 help the processor to determine the module's assignment.

5.45 Interrupt Control

5.46 As part of its initialization routine the processor enables the interrupt control with a command which is obeyed by all enabled modules . . . normally a module must be both enabled and activated in order to carry out any processor instruction. The interrupt controls of all enabled modules are addressed with $\overline{\text{FF62W}}$ from the module control logic.

5.47 With the interrupt control enabled, an interrupt can be generated by one of the following signals:

- $\overline{\text{PRGM INT}}$
- $\overline{\text{DATA INT}}$
- $\overline{\text{TIM INT}}$.

5.48 The interrupt control circuit consists of flip-flops which store the $\overline{\text{PRGM INT}}$, $\overline{\text{DATA INT}}$, and $\overline{\text{TIM INT}}$ signals as well as the interrupt enable signal. Also included in the interrupt control circuit are two one-shot timers and interrupt output gates.

5.49 The $\overline{\text{PRGM INT}}$ is latched when front panel PROGRAM switch S4 is momentarily pressed. The $\overline{\text{PRGM INT}}$ is stored in both the program interrupt and data interrupt flip-flops. When the processor is servicing this interrupt, programmable operating parameters can be reviewed and changed via the mainframe keypad (refer to Part 4). Depressing the # key on the keypad terminates the servicing of this interrupt . . . this is the only manually terminated interrupt service.

5.50 The $\overline{\text{DATA INT}}$ signal can be caused by the tone change detector and the one-shot timers as well as by the $\overline{\text{PRGM INT}}$. The $\overline{\text{DATA INT}}$ signal caused by the tone change detector indicates that a signal change (presence or absence) has occurred at one of the input ports.

5.51 When the processor determines that an input signal has appeared, it usually compares or measures the signal amplitude. In some instances it

may be necessary to delay the measurement . . . allow the signal to reach a steady state. The one-shot timers produce an 8-millisecond delay under processor control. The one-shot timer control signals are received via the interface control no. 2. Delays in signal amplitude measurement are not required with the SF Receiver so the one-shot timers are not used by this module.

5.52 A $\overline{\text{TIM INT}}$ signal is caused by a timing signal (TIMER 0, TIMER 1, or TIMER 2) received from the timer circuit in Memory and Timer A2. The received timing signal usually indicates a specified time interval has elapsed since a change occurred in the input signal from Single Frequency Input A3. The timing signals are under control of the processor.

5.53 While servicing an interrupt, the processor uses the interrupt enable flip-flop to inhibit all interrupts at the interrupt output gates. Note that the interrupt being serviced may have been requested by a module other than the SF module. Also, the program, data, or timer flip-flop storing the signal responsible for the particular interrupt being serviced, is cleared (reset) by the processor during the interrupt service routine.

5.54 Module Control Logic

5.55 The module control logic provides the following control operations:

- Enables or inhibits the interrupt control
- Activates or deactivates the module
- Decodes I/O addresses
- Resets the interrupt control flip-flops.

5.56 The module control logic consists of the module active flip-flop and I/O decoder. The module active flip-flop activates the I/O decoder, and allows the processor access to the module memory and the mapped I/O circuits. The I/O decoder determines which memory map I/O circuit is being accessed. Table G provides a general interface I/O memory map. Tables H and I detail the address codes for respective read and write operations. The tables also specify the used data bits.

5.57 The I/O decoder allows the processor to use address $\overline{\text{FF62}}$ and write $\overline{\text{MEMW}}$ pulses to enable the interrupt control during initialization routines, to inhibit the interrupt control while servicing an interrupt, and to again enable the interrupt control as part of the interrupt service routine. Note that the interrupt control circuits of all enabled modules are enabled or inhibited at the same time.

5.58 The module active flip-flop uses the $\overline{\text{MOD SET}}$ signal from Memory and Timer A2 to set the state of the $\overline{\text{MOD ACT}}$ signal low or high as determined by data bit D0. A low $\overline{\text{MOD SET}}$ occurs only during a $\overline{\text{MEMW}}$ pulse and indicates that:

- Block 4XXX is being addressed and the ENABLE A switch is latched on
- Block 5XXX is being addressed and the ENABLE B switch is latched on
- Block 6XXX is being addressed and the ENABLE SUPV switch is latched on.

5.59 A low $\overline{\text{MOD ACT}}$ activates the module, and a high $\overline{\text{MOD ACT}}$ deactivates the module. The processor has full access to the module while $\overline{\text{MOD ACT}}$ is low.

TABLE G

INTERFACE MAPPED I/O CODES

ADDRESS	DATA BITS USED	FUNCTION
WRITE		
$\overline{\text{FF60}}$	D3-D5	Write to data, timer, and program flip-flops (U15A, U14B, and U21)
$\overline{\text{FF62}}$	D0	Write to interrupt enable flip-flop (U15B)
$\overline{\text{FF64}}$-$\overline{\text{FF67}}$	D0-D7	Write to programmable peripheral interface no. 2 (PPI 2)
$\overline{\text{FF68}}$-$\overline{\text{FF6B}}$	D0-D7	Write pulse to Memory and Timing circuit card A2
$\overline{\text{FF6C}}$-$\overline{\text{FF6F}}$	D0-D7	Write to programmable peripheral interface no. 1 (PPI 1)
READ		
$\overline{\text{FF64}}$-$\overline{\text{FF67}}$	D0-D7	Read from programmable peripheral interface no. 2 (PPI 2)
$\overline{\text{FF68}}$-$\overline{\text{FF6B}}$	D0-D7	Read from Memory and Timer circuit card A2
$\overline{\text{FF6C}}$-$\overline{\text{FF6F}}$	D0-D7	Read from programmable peripheral interface no. 1 (PPI 1)

TABLE H

DIGITAL INTERRUPT AND INTERFACE A1 WRITE COMMANDS

ADDRESS	DATA BITS 7	6	5	4	3	2	1	0	DESCRIPTION
$\overline{FF60}$					1				Sets program flip-flop U21A
$\overline{FF60}$				1					Sets data interrupt flip-flop U15A
$\overline{FF60}$			1						Sets timer interrupt flip-flop U14
$\overline{FF61}$	NOT APPLICABLE								Illegal command
$\overline{FF62}$								1	Sets interrupt enable flip-flop U15B
$\overline{FF63}$	NOT APPLICABLE								Illegal command
$\overline{FF64}$	ALL								Set D/A U3 level . . . negative logic
$\overline{FF65}$	NOT APPLICABLE								Illegal command
$\overline{FF66}$								1	Triggers L2L one-shot U9
$\overline{FF66}$							0		Disables L2L one-shot U9
$\overline{FF66}$						1			Triggers L1L one-shot U9
$\overline{FF66}$					0				Disables L1L one-shot U9
$\overline{FF67}$	ALL								Control for PPI 2 U3
$\overline{FF68}$ Through $\overline{FF6B}$	ALL								Control words for Memory and Timer circuit card A2
$\overline{FF6C}$								1	Tone 0 present
$\overline{FF6C}$							1		Tone 1 present
$\overline{FF6C}$						1			Tone 2 present
$\overline{FF6C}$					1				Tone 3 present
$\overline{FF6C}$				1					Tone 4 present
$\overline{FF6C}$			1						Tone 5 present
$\overline{FF6C}$		1							Tone 6 present
$\overline{FF6C}$	1								Tone 7 present
$\overline{FF6D}$	NOT APPLICABLE								Illegal command
$\overline{FF6E}$								1	Enable Line 1
$\overline{FF6E}$							1		Enable Line 2
$\overline{FF6E}$						1			Program lamp control . . . negative logic
$\overline{FF6E}$					1				Module status . . . negative logic
$\overline{FF6F}$	ALL								Control word for PPI 1 U7
	BLANK = DON'T CARE								

Not used by the 2760-17 module

TABLE I

DIGITAL INTERRUPT AND INTERFACE A1 READ COMMANDS

ADDRESS	DATA BITS 7	6	5	4	3	2	1	0	DESCRIPTION
$\overline{FF60}$ Through $\overline{FF63}$	NOT APPLICABLE								Illegal command
$\overline{FF64}$	ALL								Current D/A setting
$\overline{FF65}$								1	Status of ENABLE B switch
$\overline{FF65}$							1		Status of ENABLE B switch
$\overline{FF65}$						1			Status of ENABLE SUPV switch
$\overline{FF65}$					1				Status of program flip-flop
$\overline{FF65}$				1					Status of data flip-flop
$\overline{FF65}$			1						Status of timer 0
$\overline{FF65}$		1							Status of timer 1
$\overline{FF65}$	1								Status of timer 2
$\overline{FF66}$								1	Trigger status of L2L one-shot
$\overline{FF66}$							0		Enable status of L2L one-shot . . . negative logic
$\overline{FF66}$						1			Trigger status of L1L one-shot
$\overline{FF66}$					0				Enable status of L1L one-shot . . . negative logic
$\overline{FF66}$				1					Enable L1L one-shot output . . . negative logic
$\overline{FF66}$			1						Enable L2L one-shot output . . . negative logic
$\overline{FF66}$		1							Status of L2L line
$\overline{FF66}$	1								Status of L1L line
$\overline{FF67}$	ALL								PPI 2 control word status
$\overline{FF68}$ Through $\overline{FF6B}$	ALL								Status of control words from Memory and Timer circuit card A2.
$\overline{FF6C}$								1	Status of TP0 tone present
$\overline{FF6C}$							1		Status of TP1 tone present
$\overline{FF6C}$						1			Status of TP2 tone present } Not used by the 2760-17 module
$\overline{FF6C}$					1				Status of TP3 tone present
$\overline{FF6C}$				1					Status of TP4 tone present
$\overline{FF6C}$			1						Status of TP5 tone present
$\overline{FF6C}$		1							Status of TP6 tone present
$\overline{FF6C}$	1								Status of TP7 tone present
$\overline{FF6D}$								1	TD0 tone detect
$\overline{FF6D}$							1		TD1 tone detect
$\overline{FF6D}$						1			TD2 tone detect } Not used by the 2760-17 module
$\overline{FF6D}$					1				TD3 tone detect
$\overline{FF6D}$				1					TD4 tone detect
$\overline{FF6D}$			1						TD5 tone detect

TABLE I (Cont)

ADDRESS	DATA BITS									DESCRIPTION
		7	6	5	4	3	2	1	0	
$\overline{FF6D}$			1							TD6 tone detect } Not used by the 2760-17 module
$\overline{FF6D}$		1								TD7 tone detect }
$\overline{FF6E}$									1	Enable 1 status
$\overline{FF6E}$								1		Enable 2 status
$\overline{FF6E}$							1			Program lamp status . . . negative logic
$\overline{FF6E}$						1				Mode switch A status . . . negative logic
$\overline{FF6E}$					1					Mode switch B status . . . negative logic
$\overline{FF6E}$				1						Mode switch C status . . . negative logic
$\overline{FF6E}$		1								Mode switch D status . . . negative logic
$\overline{FF6F}$									1	PPI 1 control word status
	BLANK = DON'T CARE									

5.60 Tone Change Detector and Interface Control No. 1

5.61 Processed input signals from Single Frequency Input A3 are applied as tone data inputs (TD1-TD7) to the tone change detector and interface control no. 1. Only tone data TD0 and TD1 are used by the SF Receiver module.

5.62 The tone change detector compares tone data inputs TD0-TD7 with tone present inputs TP0-TP7 from interface control no. 1. During initialization, TP0-TP7 are set low. A $\overline{\text{DATA INT}}$ signal is applied to the interrupt control each time a difference between the two sets of inputs (tone data and tone present) is observed. The TP0-TP7 lines are set to the same bit pattern as the TD0-TD7 bit pattern by a service routine. This results in two $\overline{\text{DATA INT}}$ signals being generated for each detected tone burst . . . one signal for the start of the tone burst, and another signal for the end of the tone burst.

5.63 Interface control no. 1 operates as a general input/output device with its specific functional configuration determined by program control. After interface control no. 1 is first set with a RESOUT signal (an inverted $\overline{\text{RESOUT}}$ signal), interface ports A, B, and C are individually defined for input or output operations.

5.64 Also, control switch S5 provides for interface control no. 1 to be set for special functional modes assignable to some modules. Specifically for the SF Receiver, switch S5 controls the initial setup for the mode 1 address display and specifies if the module expects to receive delay dialing or wink supervision (refer to Part 4).

5.65 The processor uses interface control no. 1 to control some of the memory mapped I/O circuits. A write command (consisting of an address, the $\overline{\text{MEMW}}$ pulse, and data) is applied at interface control no. 1 to start an I/O circuit operation, or to provide the circuit with data. A read command (consisting of an address and $\overline{\text{MEMR}}$ pulse) is applied at the interface control to pass results and/or status data from the circuit to the data bus.

5.66 Level Measure and Interface Control No. 2

5.67 Processed signal level data from Single Frequency Input A3 is applied as dc line level inputs L1L and L2L to the level measure. Level measure operations are controlled by interface control no. 2.

5.68 The level measure circuit consists of an eight-bit D-to-A (digital-to-analog) converter and two voltage comparators. The converter changes the eight-bit input to a voltage level proportional to the digital input value. The comparators determine if the input signal level is above or below the threshold level set by the output of the converter. With the exception of interrupt service routines, the digital input value is set for a minimum limit which the input signal level must exceed to be considered a valid signal.

5.69 For Single Frequency Input A3, L1L and L2L are determined from input signal levels provided by wideband prefilter circuits; therefore, L1L

and L2L are proportional to the total energy of the received voice frequencies. When this energy level exceeds the minimum limit set at the threshold input to the comparator, the appropriate L1 or L2 indicator on the front of the module lights up.

5.70 While servicing an interrupt, the processor may require more specific information about the signal level than that determined by the minimum threshold limit. The additional information required depends on the module's display mode (refer to Part 4). For mode 1, the processor needs only to know if the input signal exceeds the lower limit. For modes 2 and 3, the processor must compare the input signal level with minimum, lower, upper, and maximum limits to determine between which two of these limits the input signal level falls in. (In mode 3, signal level data is not displayed, but the mode 2 signal level data can be viewed by use of the scroll/cursor control located on the 2760 mainframe.)

5.71 Interface control no. 2 operates in the same manner as interface control no. 1 . . . as a general I/O device with a functional configuration determined by the processor. Interface control no. 2 passes data to and from the level measure circuit as well as to and from the interrupt control. It also transfers the state of the front panel switches (with the exception of the PROGRAM switch) and the state of the timer signals (TIMER 0, TIMER 2, and TIMER 3 from Memory and Timer A2) to the processor.

5.72 MEMORY AND TIMER A2

5.73 As shown in Fig. 25 in Part 7, the memory and timer circuit card consists of the following sections:

- Function ROM memory
- Module ROM and RAM memory
- Memory control logic
- Timer.

5.74 Function ROM Memory

5.75 The function ROM memory is divided into three sections . . . one section for an A direction receiver (ENABLE A), one section for a B direction receiver (ENABLE B), and one section for a supervision receiver (ENABLE SUPV).

5.76 The program routines contained within the function ROM Memory instruct the processor to:

- Activate the module memory
- Call the appropriate program routines stored within the module memory
- Deactivate the module memory when it is no longer required.

5.77 The positions of the front panel switches determine if the function ROM memory can respond when the address bus contains a location assigned to the function ROM memory.

5.78 Module ROM and RAM Memory

5.79 Each module has a block of ROM memory (C000 through EFFF) which contains the program routines specifically tailored to the operation of that module. A block of RAM memory (F000 through F1FF) provides storage for data.

5.80 More than one module may be enabled at the same time, but two modules cannot be enabled for the same function at the same time . . . only one module can be enabled as a supervision receiver. For example, each module uses the same ROM and RAM memory blocks. Therefore, as each module performs its assigned tasks, the module memory must be activated and deactivated by $\overline{\text{MOD ACT}}$.

5.81 Memory Control Logic

5.82 The memory control logic decodes the memory addresses and determines which memory to enable. To read from a function ROM memory location, the appropriate module function must be enabled (ENABLE A, ENABLE B, or ENABLE SUPV switch latched on) and the appropriate address block must be requested. In addition to these two requirements, to read from the module ROM memory location and to read or write from a module RAM location requires that the module be activated ($\overline{\text{MOD ACT}} = 0$).

5.83 The control logic also provides two signals (MEMR and MEMR[1]). These signals allow the data to flow from the module to the system data bus. Normally, the data flow is from the data bus into the module.

5.84 The control logic produces one other signal ($\overline{\text{MOD SET}}$), which in conjunction with a circuit on the digital interrupt and interface circuit card activates or deactivates the module memory.

5.85 The memory control logic (Fig. 26 in Part 7) consists of the module enable decoder, memory decoder, and MEMR delay circuits.

5.86 The memory decoder determines which memory block is being accessed . . . which particular memory circuit to select. Tables J and K list the read/write address blocks and the corresponding memory circuits. See Fig. 22 for memory circuit locations.

5.87 Prior to calling program routines located in the module memory, the processor must activate the memory. After returning from a program routine, the processor must then deactivate the module memory. Routines located in the module ROM memory may require data to be stored or retrieved from the module RAM memory.

5.88 The enable decoder senses the presence of a write instruction to a function memory and outputs a $\overline{\text{MOD SET}}$ if the module is appropriately enabled . . . for example: a 4XXX address block, ENABLE A on, and a $\overline{\text{MEMW}}$ pulse. The $\overline{\text{MOD SET}}$ pulse goes to the digital interrupt and interface circuit where it sets $\overline{\text{MOD ACT}}$ low if data bit D0 = 1, and resets $\overline{\text{MOD ACT}}$ high if data bit D0 = 0.

5.89 The MEMR delay circuit applies MEMR and MEMR[1] to the digital interrupt and interface circuit. These signals gate the data from the module into the system bus. Data from the module goes to the processor via the system bus during the following read instructions:

- Mapped I/O read instruction . . . address block FF6X
- Function ROM memory read instruction . . . address block 4XXX, 5XXX, or 6XXX and ENABLE A, ENABLE B, or ENABLE SUPV on
- Module ROM memory read instruction . . . address blocks CXXX, DXXX, or EXXX if $\overline{\text{MOD ACT}}$ = 0
- Module RAM memory read instruction . . . address blocks F0XX or F1XX if $\overline{\text{MOD ACT}}$ = 0.

5.90 Timer

5.91 The timer function provides three independently programmable interval timers. The operation of each interval timer is under the direction of the program. Decoding of the instructions and control of the timers is done by the digital interrupt and interface card.

5.92 The basic operation of an interval timer consists of loading the timer with a value equal to the required interval. The timer, using the 10-kHz clock, counts down to zero. At that instant, the counter output (TIMER 0, TIMER 1, or TIMER 2) goes high. The interval timer output goes to the digital interrupt and interface circuit where it generates an interrupt. The interrupt informs the processor that the specified interval has elapsed.

TABLE J

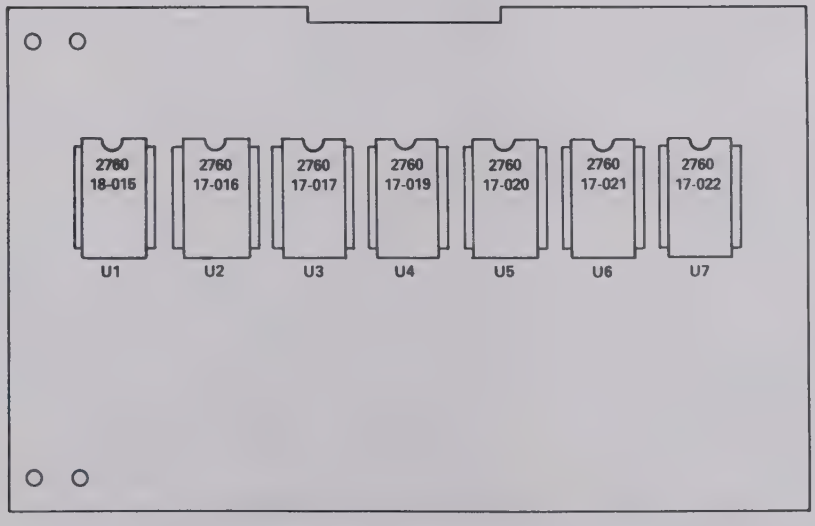
MEMORY READ COMMANDS

ADDRESS	DATA BITS 7 6 5 4 3 2 1 0	DESCRIPTION
$\overline{4000}$ Through $\overline{40FF}$	ALL	A Display ROM U1
$\overline{5000}$ Through $\overline{50FF}$	ALL	B Display ROM U1
$\overline{6000}$ Through $\overline{60FF}$	ALL	Supervision Display ROM U1
$\overline{C000}$ Through $\overline{C7FF}$	ALL	Module ROM U2
$\overline{C800}$ Through $\overline{CFFF}$	ALL	Module ROM U3
$\overline{D000}$ Through $\overline{D7FF}$	ALL	Module ROM U4
$\overline{D800}$ Through $\overline{DFFF}$	ALL	Module ROM U5
$\overline{E000}$ Through $\overline{E7FF}$	ALL	Module ROM U6
$\overline{E800}$ Through $\overline{EFFF}$	ALL	Module ROM U7
$\overline{F000}$ Through $\overline{F0FF}$	ALL	Module RAM U13, U15
$\overline{F100}$ Through $\overline{F1FF}$	ALL	Module RAM U8, U14
$\overline{FF68}$	ALL	Read timer 1 status
$\overline{FF69}$	ALL	Read timer 2 status
$\overline{FF6A}$	ALL	Read timer 3 status

TABLE K

MEMORY WRITE COMMANDS

ADDRESS	DATA BITS 7 6 5 4 3 2 1 0	DESCRIPTION
$\overline{4000}$ Through $\overline{40FF}$	1	Causes $\overline{\text{MOD ACT}}$ to activate module memory if D0 = 1, or to deactivate module memory if D0 = 0.
$\overline{5000}$ Through $\overline{50FF}$	1	Causes $\overline{\text{MOD ACT}}$ to activate module memory if D0 = 1, or to deactivate module memory if D0 = 0.
$\overline{6000}$ Through $\overline{60FF}$	1	Causes $\overline{\text{MOD ACT}}$ to activate module memory if D0 = 1, or to deactivate module memory if D0 = 0.
$\overline{F000}$ Through $\overline{F0FF}$	ALL	Module RAM U13, U15
$\overline{F100}$ Through $\overline{F1FF}$	ALL	Module RAM U8, U14
$\overline{FF68}$	ALL	Write data to timer 1(U10)
$\overline{FF69}$	ALL	Write data to timer 2 (U10)
$\overline{FF6A}$	ALL	Write data to timer 3 (U10)
$\overline{FF6B}$	ALL	Write control word to timer (U10)



PROM	MEMORY LOCATIONS (HEX)
U1	4000 - 40FF 5000 - 50FF 6000 - 60FF
U2 U3	C000 - C7FF C800 - CFFF
U4 U5	D000 - D7FF D800 - DFFF
U6 U7	E000 - E7FF E800 - EFFF

A02407-01

Fig. 22—Memory and Timer A2 ROM Address Locations

6. MAINTENANCE

A. General

6.01 This part contains information needed to maintain and align the Model 2760-17 SF Receiver module.

6.02 The following paragraphs provide a complete set of adjustment procedures required to align the module. These procedures can be used for periodic maintenance and repair checks. Table L lists the test equipment required. Personnel performing these procedures must be familiar with the test equipment recommended. ***No attempt to adjust the module should be made without proper test equipment or qualified personnel.***

6.03 Alignment of the module is presented as a series of adjustment procedures for easy reference. Alignment must be performed in the exact sequence presented as adjustment steps are often dependent on previously performed adjustments. Also, the procedures assume switch and control positions remain as set unless specific instructions require new positions.

> ***Caution: Ensure that the mainframe POWER switch is placed off when either removing or replacing extenders or boards. Failure to do so can result in damage to the receiver.***

TABLE L

REQUIRED ALIGNMENT TEST EQUIPMENT

EQUIPMENT	USE
Signal generator with an output referenced to 600 ohms.	To supply continuous sinusoidal and tone burst test signals with a dial accuracy of 1 Hz
Frequency counter	To measure audio frequencies with a resolution of 0.1 Hz
RMS ac voltmeter	To measure signal levels with a resolution of 0.1 dB referenced to 600 ohms.
Digital dc voltmeter	To measure signal levels with a resolution of 1 millivolt
Dual-trace oscilloscope	To display waveforms for time-delay and duty cycle measurements
Mainframe Extender Board* (NSSD part number C2760-00-027)	To make test points and potentiometers easily accessible
*This extender board is supplied with the 2760 mainframe.	

B. Service Information

6.04 Complete warranty information is contained in the purchase order agreement under terms and conditions of sale. Briefly, Network Support Systems products are warranted to the original purchaser for one year from the date of shipment.

6.05 If a product fails to perform as expected, call our Factory Service Center in Concord, New Hampshire at (603) 224-6511 for assistance.

6.06 Should it be necessary to return a product, a Return Material Authorization (RMA) Number is needed to track your repair order. RMA numbers are issued by Service Center Personnel.

6.07 Equipment returned for repair must be accompanied by the following information:

- Purchase Order number (if out of warranty)
- Bill-to address (if out of warranty)
- Ship-to address
- Description of the problem.

C Preparation for Alignment

6.08 Perform the following steps:

STEP	PROCEDURE
1	Set the mainframe POWER switch off.
2	Remove the SF module from the mainframe to expose test points and potentiometers located on the Single Frequency Input circuit.
3	Insert the mainframe extender board into the mainframe and plug the SF module into the extender.
4	Place a nonconductive support under the extended module to secure the connection between the module and the extender. ***Failure to provide this support can result in erratic operation of the module.***
5	Connect the frequency generator, frequency counter, and ac voltmeter as shown in Fig. 23. Ensure that the 600-ohm terminating load is present, or is provided for by the output impedance of the signal generator or frequency counter, and that input ports L1 and L2 are connected in parallel as shown.
6	Place all test equipment and mainframe power control switches on.
7	Set the signal generator for a continuous sinusoidal output of 2600 ± 0.1 Hz at 0.0 ± 0.2 dBm.
8	Depress and latch the ENABLE A pushbutton located on the front of the module.

6.09 See Figures 29 and 33 in Part 7 for the location of designated potentiometers and test points.

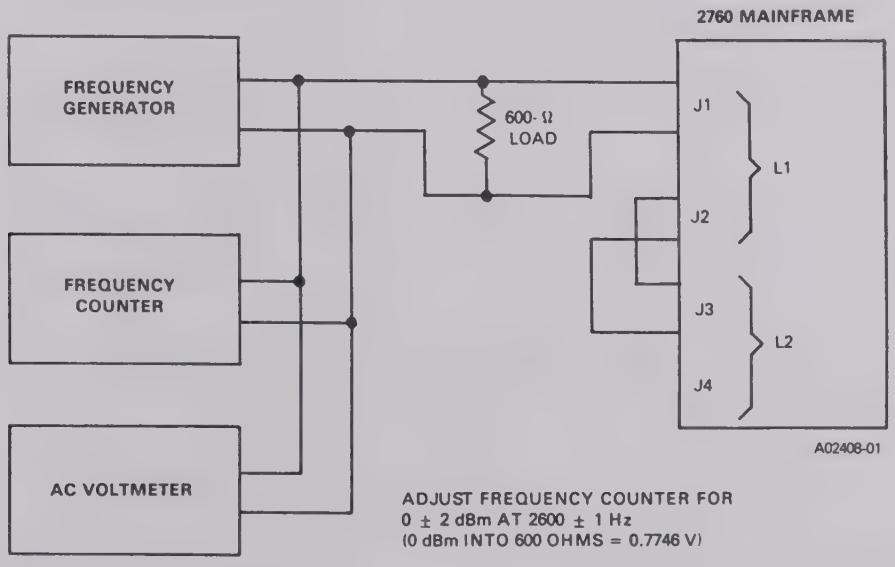


Fig. 23—Initial Test Setup

D. Alignment Procedure

6.10 Notch Filter Adjustment

STEP	PROCEDURE
1	Connect the ac voltmeter across test points TPN1 and TP1 (GND) on the Single Frequency Input Board.
2	Adjust potentiometer NF1 (R43) to obtain a null indication on the voltmeter.
3	Connect the ac voltmeter across test points TPN2 and TP1 (GND).
4	Adjust potentiometer NF2 (R143) to obtain a null indication on the voltmeter.

6.11 Center Frequency Adjustment

STEP	PROCEDURE
1	Ensure that switch S1 is in the OFF position. *Note:* Switch S1 is factory set to the OFF position and must remain in the OFF position to ensure proper operation of Single Frequency Input A3.
2	Connect the oscilloscope to test points TPF1 and TP1 (GND) for Vdc level display.
3	Adjust potentiometer F1 (R44) for a maximum Vdc level display.
4	Connect the oscilloscope to test points TPF2 and TP2 (GND) for a Vdc level display.
5	Adjust potentiometer F2 (R144) for a maximum Vdc level display.

6.12 Response Time Adjustment

STEP	PROCEDURE
1	Use channel 1 of the oscilloscope to obtain a display of the input signal at the L1/L2 mainframe jack ports.
2	Without changing frequency or voltage levels, set the signal generator for a tone burst output of 50 msec on and 100 msec off as shown in Fig. 24.
3	Connect channel 2 of the oscilloscope to the right side of resistor R30 (see TD0 in Fig. 26 in Part 7) to obtain a time response display as shown in Fig. 24.
4	Adjust potentiometer PW1 to set T_{ON} equal to 10 ± 0.5 msec.
5	Connect channel 2 of the oscilloscope to the right side of resistor R130 (see TD1 in Fig. 26 in Part 7) to obtain a time response display.
6	Adjust potentiometer PW2 to set T_{ON} equal to 10 ± 0.5 msec.
7	Set the mainframe power control switch to off.
8	Remove all oscilloscope and ac voltmeter test probes from the Single Frequency Input circuit.

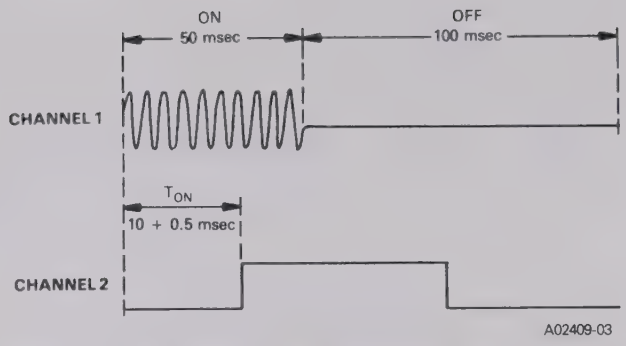


Fig. 24—Tone Burst and Response Time Display

6.13 Level Measure Adjustment

STEP	PROCEDURE
1	Remove the top two screws which hold the Single Frequency Input and the Memory and Timer circuit cards adjacent to the Digital Interrupt and Interface circuit card. Lower the board sandwich to expose the Digital Interrupt and Interface circuit components.
2	Set the frequency generator for a continuous sinusoidal output of 1700 ± 10 Hz at −26 ± 1 dBm.
3	Connect the digital dc voltmeter between the left side of resistor R29 and the standoff labeled "M" on the Digital Interrupt and Interface circuit.
4	Set the volume control on the frequency generator for a reading of 89 ± 1 millivolts on the dc meter.
5	Rotate potentiometer R4 clockwise as necessary to turn off the module's L1 and L2 LED indicators.
6	Slowly rotate potentiometer R4 counterclockwise until the L1 and L2 LED indicators are both turned on.
7	Set the mainframe and all test equipment power control switches to off.
8	Remove all test probes from the Digital Interrupt and Interface circuit. Replace the two top screws which secure all three circuit boards adjacent to one another, and restore the SF Receiver module into the mainframe.

7. DIAGRAMS

A. General

7.01 This part contains the functional, interconnections, schematics, and parts location diagrams for the 2760-17 SF Receiver.

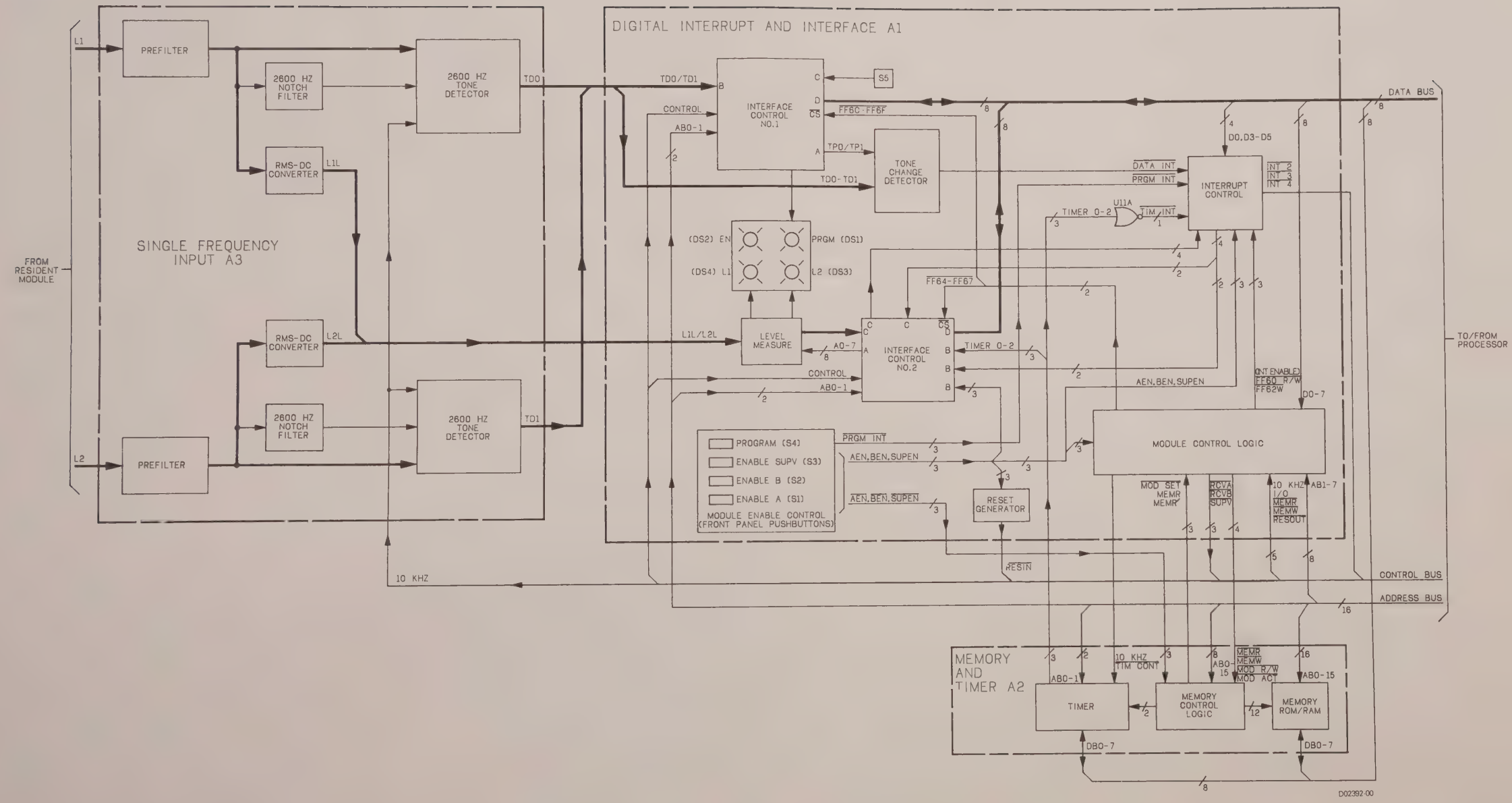


Fig. 25—SF Receiver Block Diagram

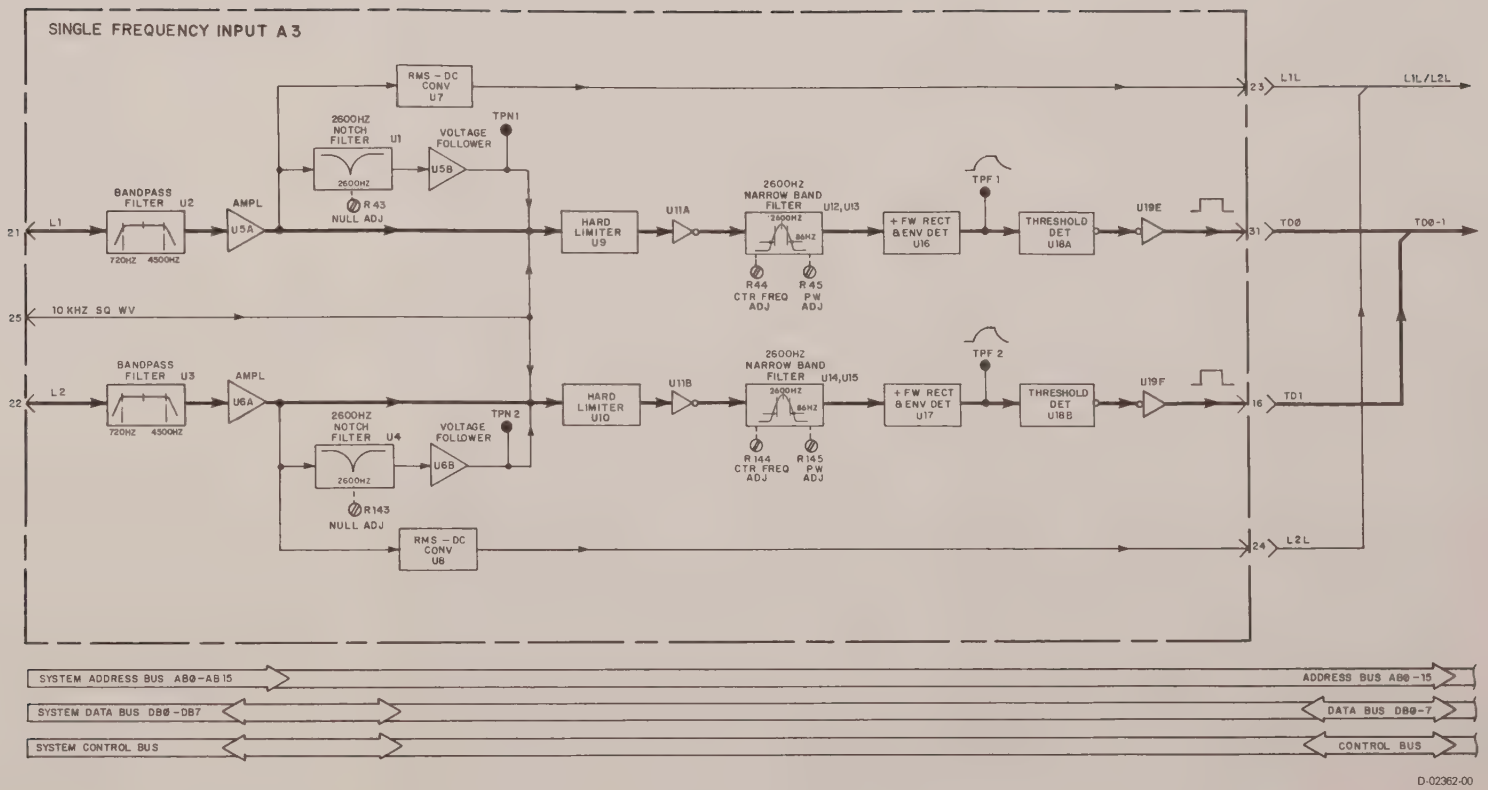


Fig. 26—SF Receiver Functional Diagram (Sheet 1 of 2)

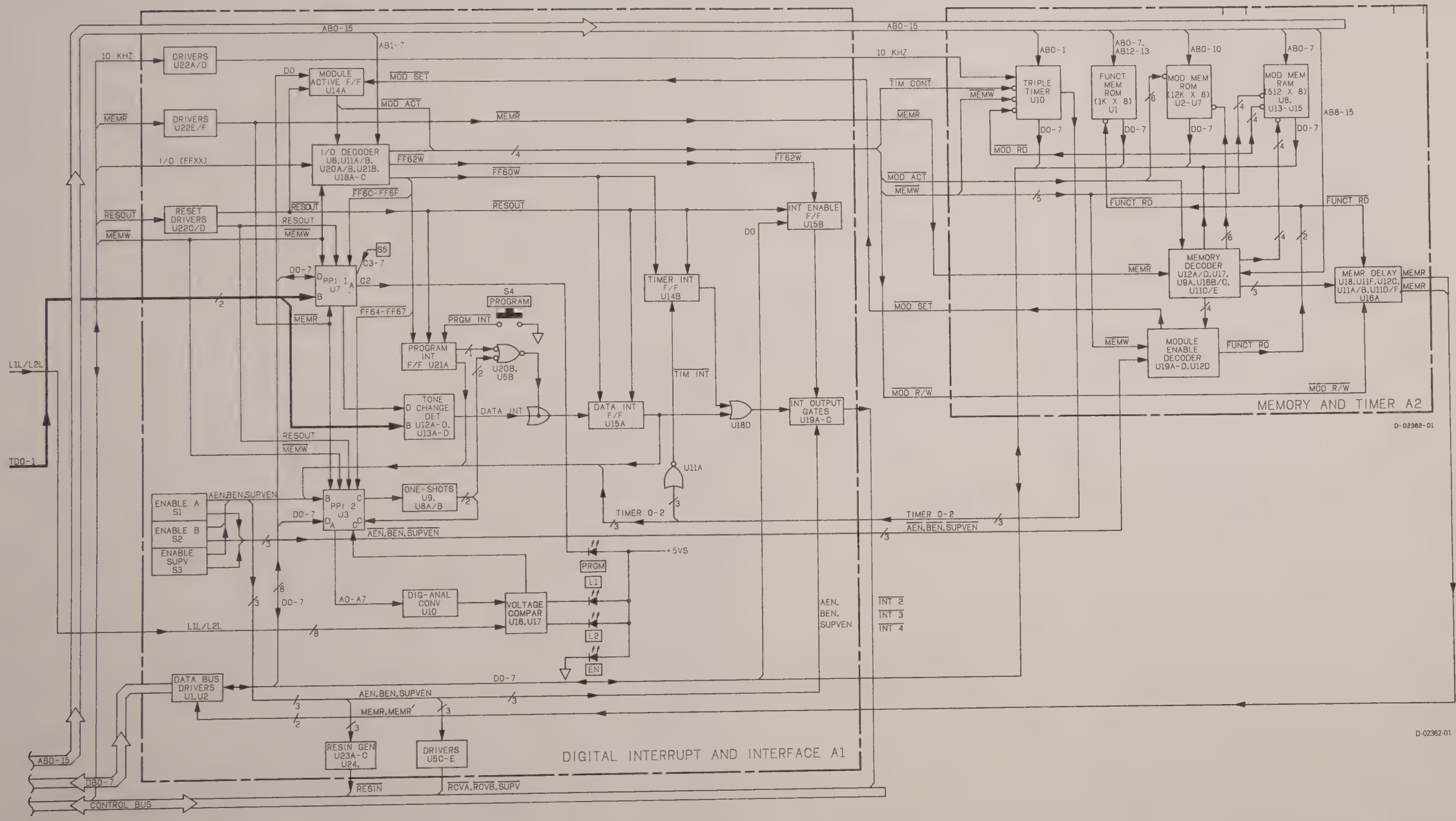
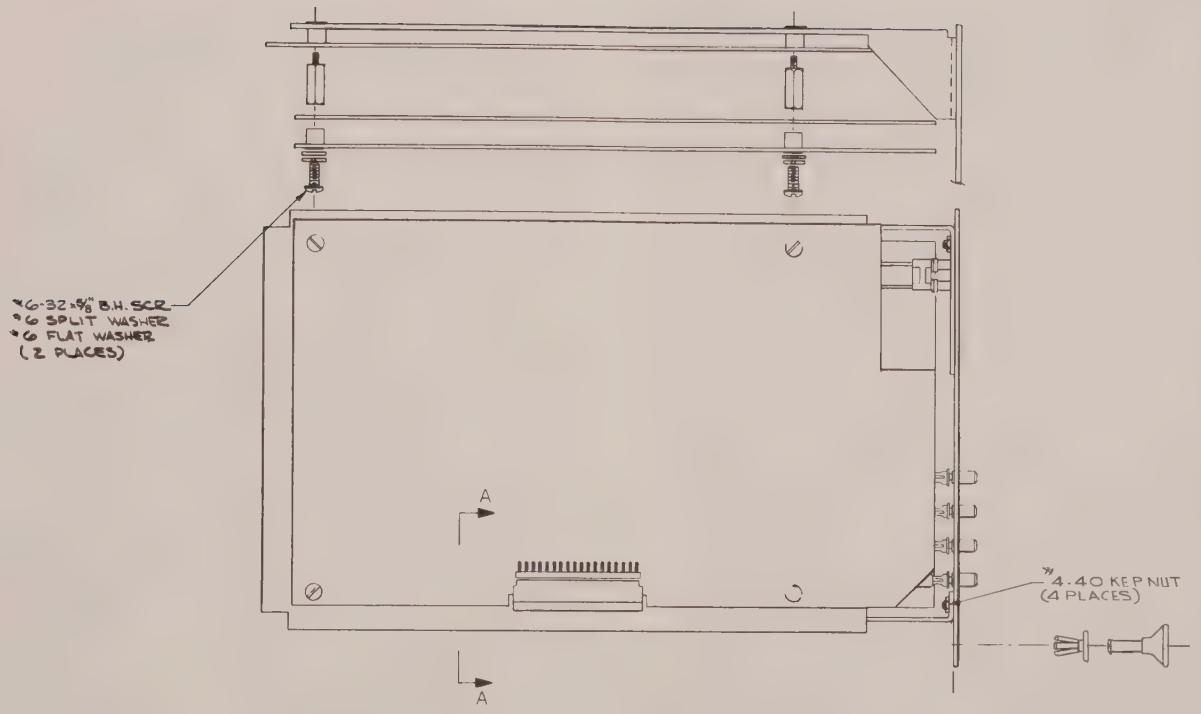
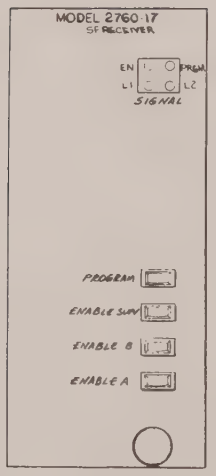
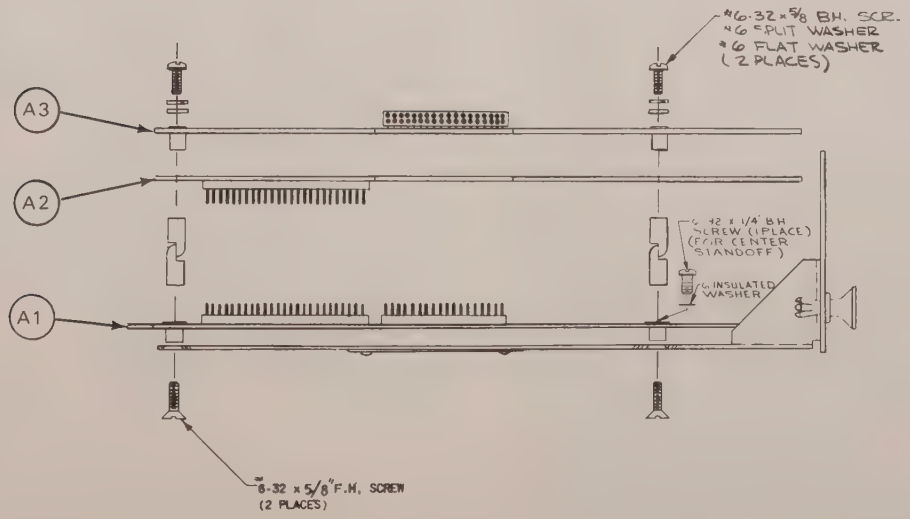


Fig. 26—SF Receiver Functional Diagram (Sheet 2 of 2)







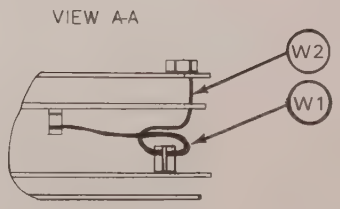


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Fig. 27—SF Receiver Overall Assembly Diagram

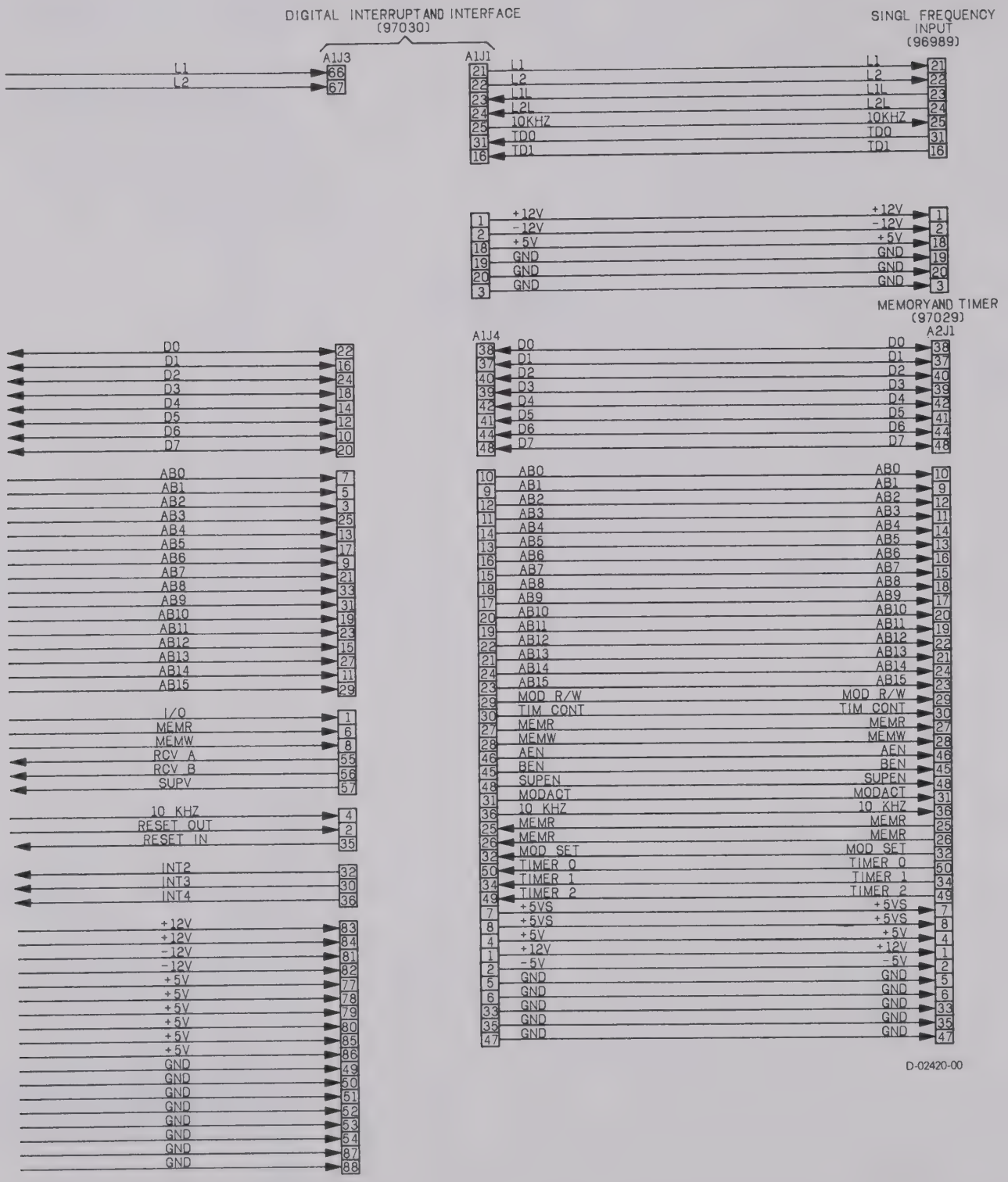


Fig. 28—SF Receiver Interconnection Diagram

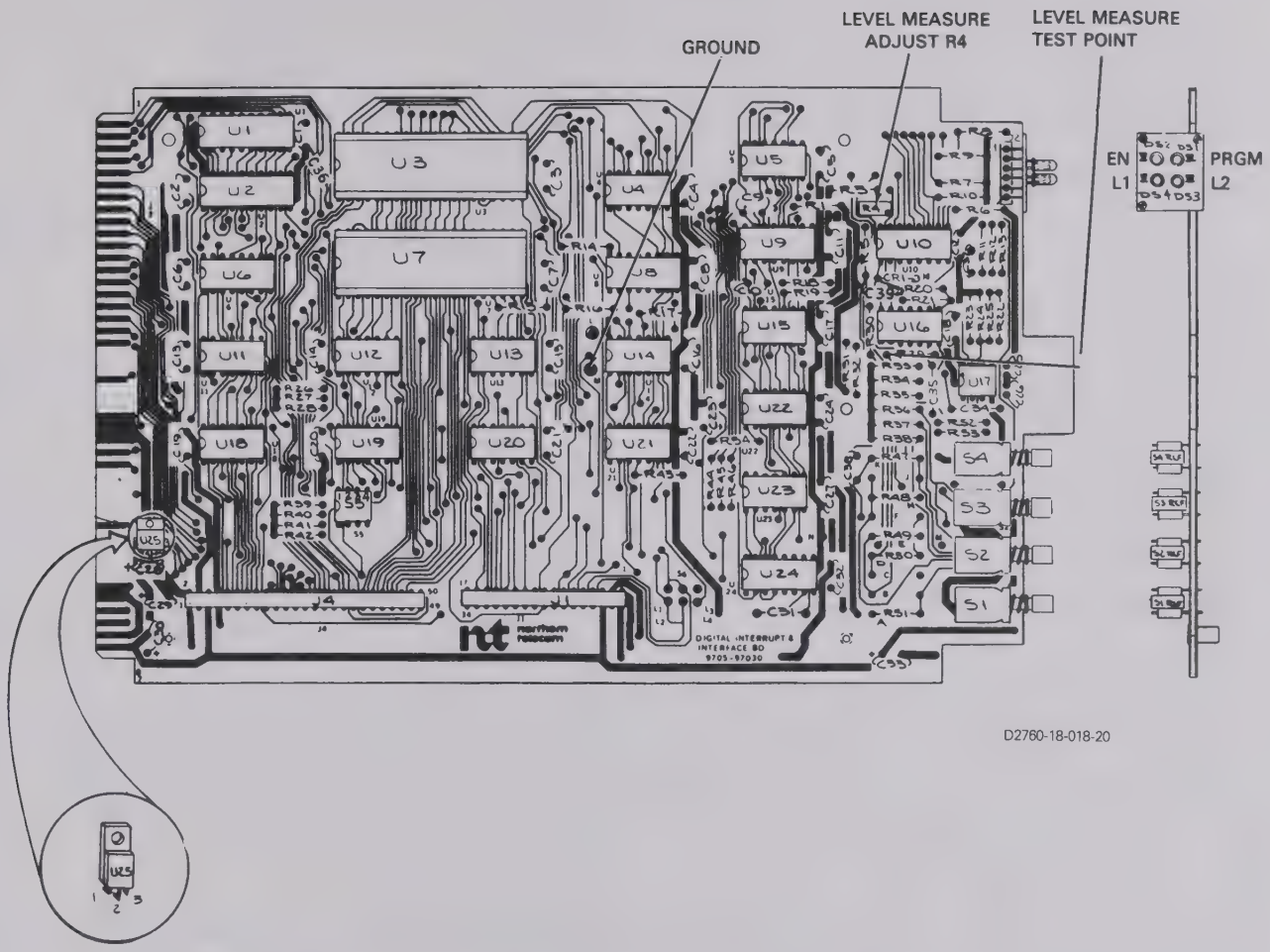
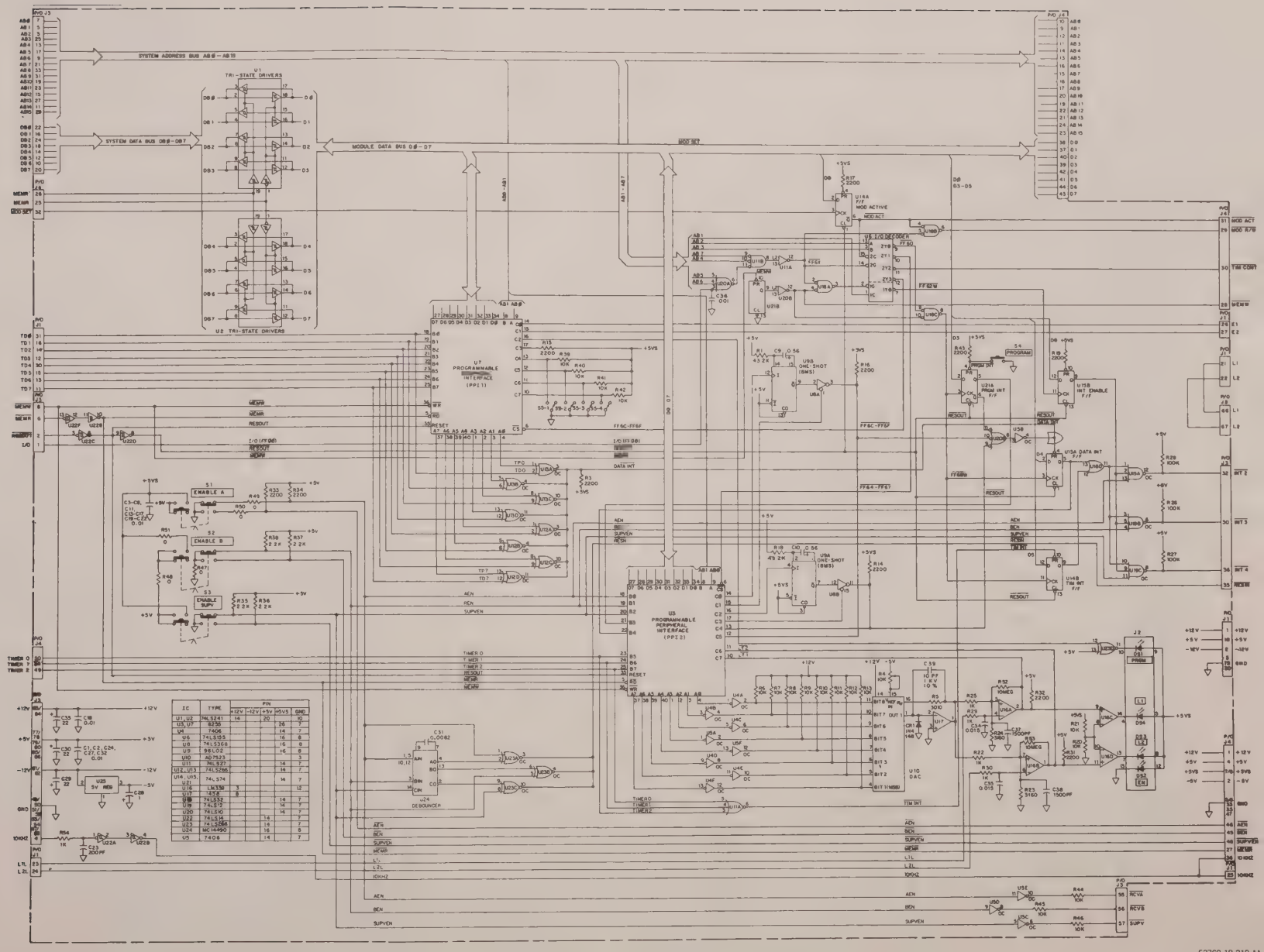


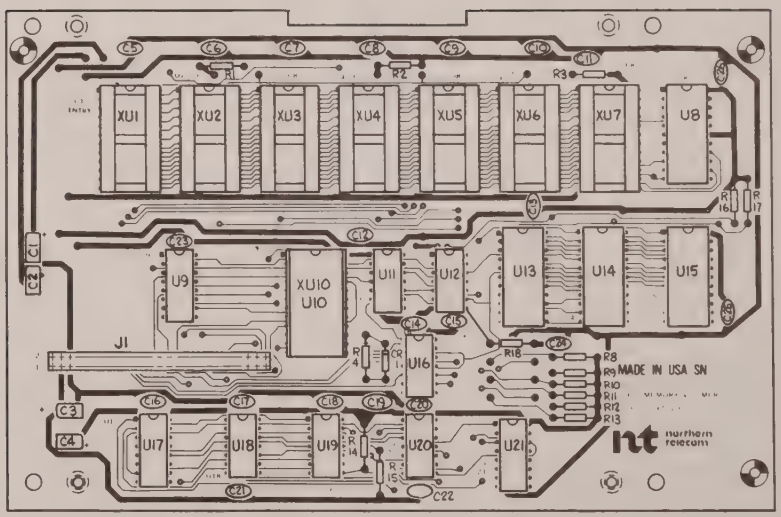
Fig. 29—Digital Interrupt and Interface (A1) Parts Location Diagram



IC	TYPE	PIN +12V	-12V	+5V	GND
U1, U2	74LS241	14		20	10
U13, U7	8255			26	7
U4	7406			14	7
U6	74LS155			16	8
U8	74LS368			16	8
U9	9580 2			16	8
U10	AD7523				3
U11	74LS27			14	7
U12, U13	74LS266			14	7
U14, U15	74L S74			14	7
U21					
U16	LM339	3			12
U17	4558	8			
U18	74LS32			14	7
U19	74LS12			14	7
U20	74LS10			14	7
U22	74LS14	14			7
U23	74 LS266	14			7
U24	MC14490			16	8
U5	7406	14			7

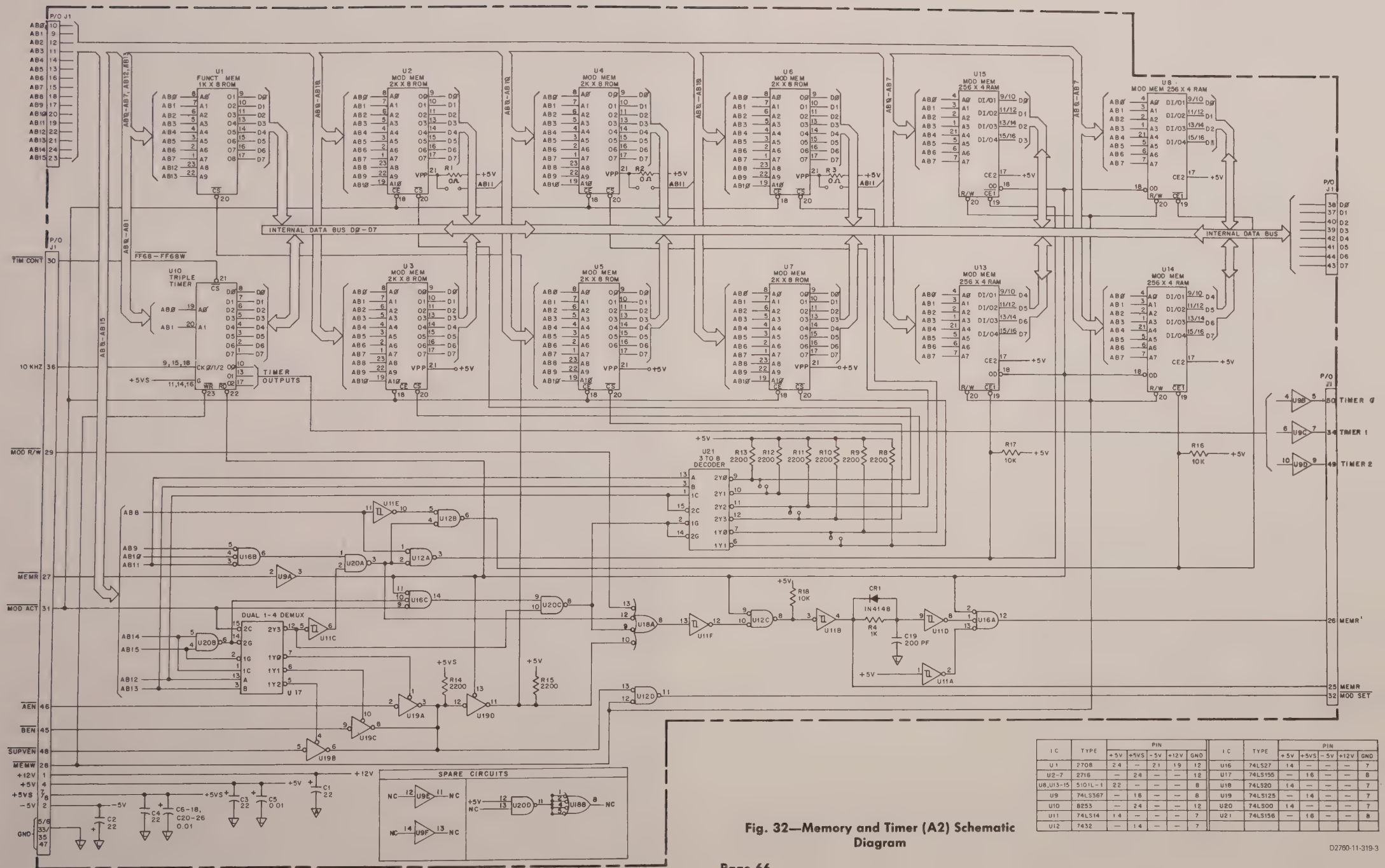
E2760-18-318-11

Fig. 30—Digital Interrupt and Interface (A1) Schematic Diagram



D2760-11-019-7

Fig. 31—Memory and Timer (A2) Parts Location Diagram

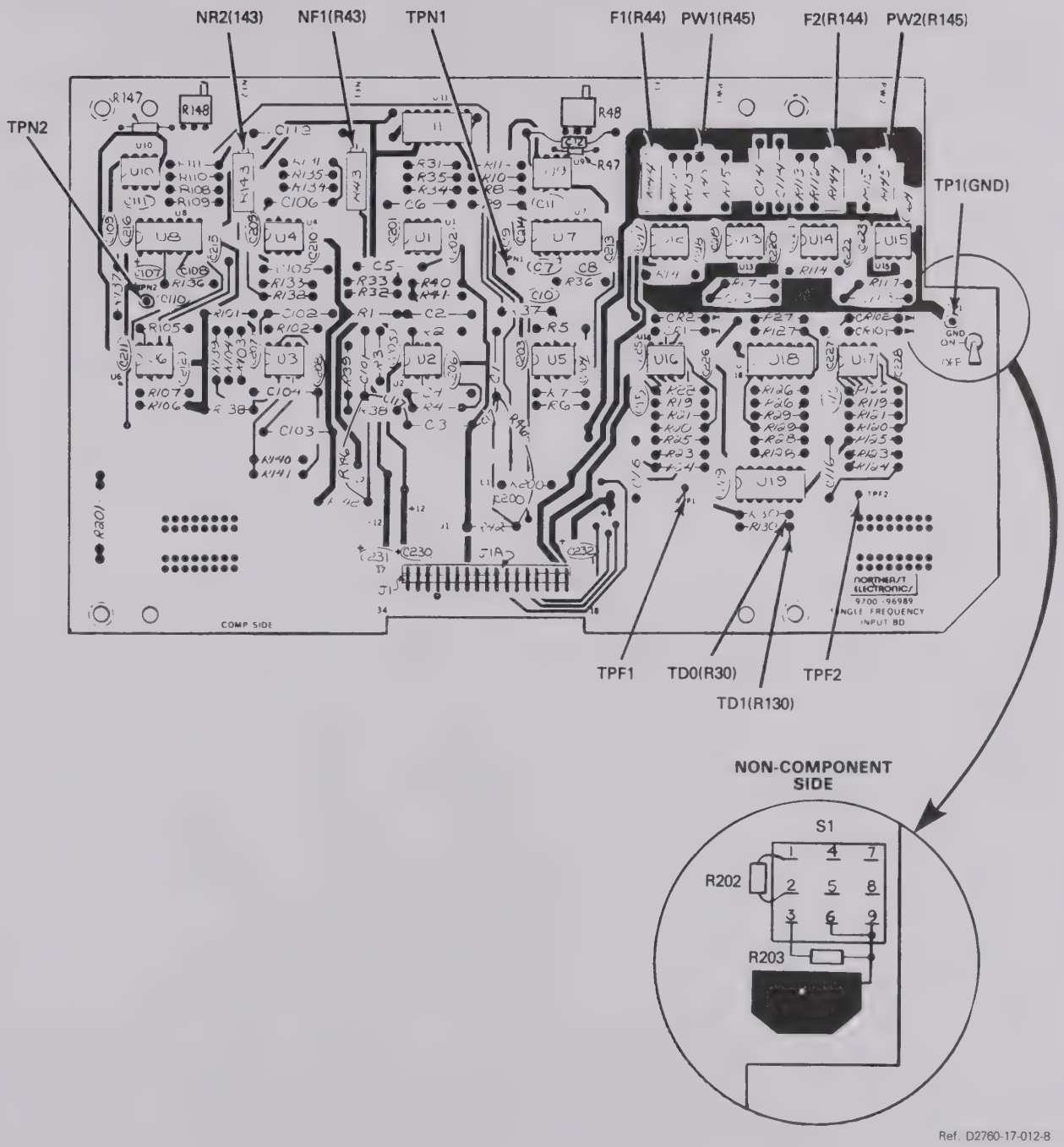


IC	TYPE	PIN				
		+5V	+5VS	-5V	+12V	GND
U1	2708	24	—	21	19	12
U2-7	2716	—	24	—	—	12
U8,U13-15	5101L-1	22	—	—	—	8
U9	74LS367	—	16	—	—	8
U10	8253	—	24	—	—	12
U11	74LS14	14	—	—	—	7
U12	7432	—	14	—	—	7

IC	TYPE	PIN				
		+5V	+5VS	-5V	+12V	GND
U16	74LS27	14	—	—	—	7
U17	74LS155	—	16	—	—	8
U18	74LS20	14	—	—	—	7
U19	74LS125	—	14	—	—	7
U20	74LS00	14	—	—	—	7
U21	74LS156	—	16	—	—	8

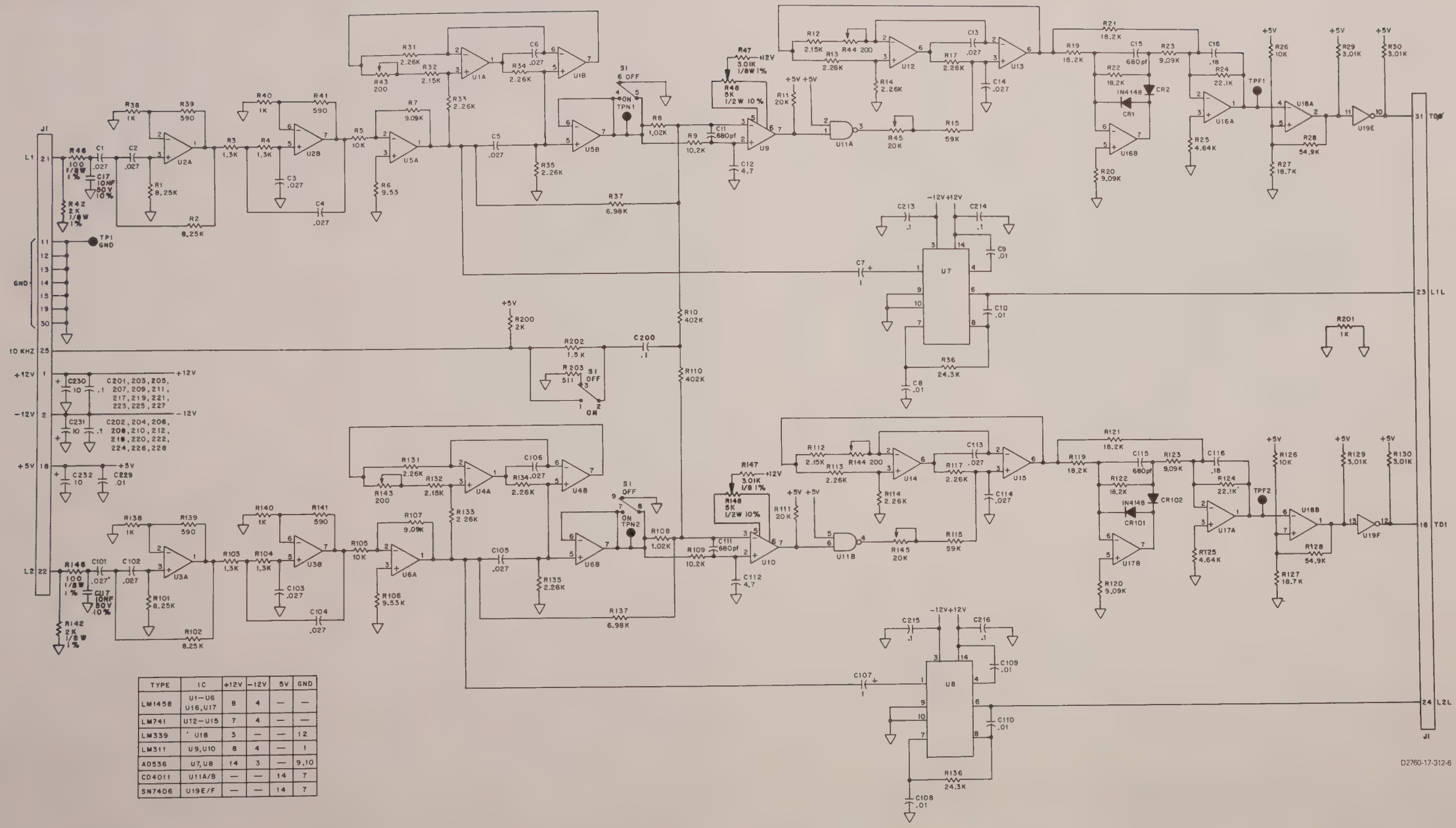
D2760-11-319-3

Fig. 32—Memory and Timer (A2) Schematic Diagram



Ref. D2760-17-012-8

Fig. 33—Single Frequency Input (A3) Parts Location Diagram



TYPE	IC	+12V	-12V	5V	GND
LM1458	U1–U6 U16,U17	8	4	—	—
LM741	U12–U15	7	4	—	—
LM339	U18	3	—	—	12
LM311	U9,U10	8	4	—	1
AD536	U7,U8	14	3	—	9,10
CD4011	U11A/B	—	—	14	7
SN7406	U19E/F	—	—	14	7

Fig. 34—Single Frequency Input (A3) Schematic Diagram

8. ELECTRONIC PARTS LISTS

A. General

8.01 This part contains the electronic parts lists for the 2760-17 SF Receiver.

TABLE M

SF RECEIVER PARTS LIST

A2760-17-001
REV 04 DATED 9/14/84

REFERENCE DESIGNATOR	DESCRIPTION	PART NO.
A1	DIGITAL INTRPT & I/F BD	A276018018
A2	MEMORY AND TIMER BD.	A276011019
A3	SINGLE FREQUENCY INPUT BD	A276017012
W1	DIGITAL CABLE ASSY	A276011021
W2	SF ANALOG CABLE ASSY	A276017010

TABLE N

DIGITAL INTERRUPT AND INTERFACE (A1) PARTS LIST

A2760-18-018
REV 20 DATED 9/14/84

REFERENCE DESIGNATOR	DESCRIPTION								PART NO.
C1-8	CAPACITR	CERAMIC	10	NF	CAP.082	F	16V	20% Y5P	330701031
C9-10	CAPACITR	ELECT-TA	560	NF	CAP.036	F	35V	10%	310005640
C11-22	CAPACITR	CERAMIC	10	NF	CAP.082	F	16V	20% Y5P	330701031
C23	CAPACITR	CERAMIC	200	PF	CAP.082	F	1KV	10% N3300	330002010
C24	CAPACITR	CERAMIC	10	NF	CAP.082	F	16V	20% Y5P	330701031
C25	CAPACITR	CERAMIC	100	NF	CAP.088	F	50V	20% Z5U	330801040
C26	CAPACITR	CERAMIC	100	NF	CAP.088	F	50V	20% Z5U	330801040
C27	CAPACITR	CERAMIC	10	NF	CAP.082	F	16V	20% Y5P	330701031
C28	CAPACITR	ELECT-TA	1.0	UF	CAP.036	F	35V	10%	310001051
C29-C30	CAPACITR	ELECT-TA	22	UF	CAP.037	F	15V	10%	310002261
C31	CAPACITR	POLYESTR	8.2	NF	CAP.043	P	100V	10%	320008220
C32	CAPACITR	CERAMIC	10	NF	CAP.082	F	16V	20% Y5P	330701031
C33	CAPACITR	ELECT-TA	22	UF	CAP.037	F	15V	10%	310002261
C34-35	CAPACITR	POLYESTR	15	NF	CAP.043	F	100V	10%	320001530
C36	CAPACITR	CERAMIC	1.0	NF	CAP.088	F	50V	10% X7R	330801021
C37-38	CAPACITR	CERAMIC	1.5	NF	CAP.093	F	1KV	10% Z5R	330001520
C39	CAPACITR	CERAMIC	10	PF	CAP.082	N	1KV	10% N330	330001000
CR1	DIODE	SIGNAL	1N4148		RES.001		75V	SI 4.0NS	560041480
J1	CONNECTR	HEADER	34	DIL	HDR17.2C		GOLD	STRAIGHT	654003319
J2	CONNECTR	HEADER	6	SIL			TIN	R-ANGLE	654003241
J4	CONNECTR	HEADER	50	DIL			GOLD	STRAIGHT	654003311
R1	RESISTOR	MTL-FILM	46.4	K	RES.001	P	.25W	1% 100PPM 250V	220246421
R3	RESISTOR	CARBON	2.2	K	RES.001	F	1/4W	10%	200102226

TABLE N (Cont)

A2760-18-018
REV 20 DATED 9/14/84

REFERENCE DESIGNATOR	DESCRIPTION							PART NO.
R4	TRIM-POT	CERM-20T	10	K	VRES.008	F	1/2W 10% TOP-ADJ	232701034
R5	RESISTOR	MTL-FILM	3.01	K	RES.001	N	.25W 1% 100PPM 250V	220230111
R6-13	RESISTOR	CARBON	10	K	RES.001	F	1/4W 10%	200101036
R14-17	RESISTOR	CARBON	2.2	K	RES.001	F	1/4W 10%	200102226
R18	RESISTOR	MTL-FILM	46.4	K	RES.001	P	.25W 1% 100PPM 250V	220246421
R19	RESISTOR	CARBON	2.2	K	RES.001	F	1/4W 10%	200102226
R20-21	RESISTOR	MTL-FILM	10.0	K	RES.001	P	.25W 1% 100PPM 250V	220210021
R22	RESISTOR	MTL-FILM	1.00	K	RES.001	P	.25W 1% 100PPM 250V	220210011
R23-24	RESISTOR	MTL-FILM	3.16	K	RES.001	P	.25W 1% 100PPM 250V	220231611
R25	RESISTOR	MTL-FILM	1.00	K	RES.001	P	.25W 1% 100PPM 250V	220210011
R26-28	RESISTOR	CARBON	100	K	RES.001	F	1/4W 10%	200101046
R29-30	RESISTOR	MTL-FILM	1.00	K	RES.001	P	.25W 1% 100PPM 250V	220210011
R31-38	RESISTOR	CARBON	2.2	K	RES.001	F	1/4W 10%	200102226
R39-42	RESISTOR	CARBON	10	K	RES.001	F	1/4W 10%	200101036
R43	RESISTOR	CARBON	2.2	K	RES.001	F	1/4W 10%	200102226
R44-46	RESISTOR	MTL-FILM	10.0	K	RES.001	P	.25W 1% 100PPM 250V	220210021
R47-51	RESISTOR	CARBON	0.0	R	RES.001	P	1/4W ZEROHM	200100001
R47-51	WIRE	JUMPER	.01-DCR			F	ZEROHM MOLDED	890200400
R52-53	RESISTOR	CARBON	10	M	RES.001	F	1/4W 10%	200101066
R54	RESISTOR	MTL-FILM	1.00	K	RES.001	P	.25W 1% 100PPM 250V	220210011
S1-S3	SWITCH	PUSH-BTN	1S2P		SW.010		EE ACTION - SPECIAL	635801300
S4	SWITCH	PUSH-BTN	1S2PDT				BLACK NON-SHRT	635800901
S5	SWITCH	DIP	4 POS		DIP.8			640001003
U1-2	INT-CKT	LS-TTL	74LS241		DIP.20.3	P	8 BUFFER /3S	510974241
U3	INT-CKT	MICRO-PR	8255		DIP.40.6		PROG PERPH INTRFCE	514001601
U4	INT-CKT	TTL	7406		DIP.14	N	HEX INV BUF DRV /OC	510074060
U5	INT-CKT	TTL	7406		DIP.14	N	HEX INV BUF DRV /OC	510074060
U6	INT-CKT	LS-TTL	74LS155		DIP.16	P	2X2TO4 DECDR/DEMUX	510974155
U7	INT-CKT	MICRO-PR	8255		DIP.40.6		PROG PERPH INTRFCE	514001601
U8	INT-CKT	LS-TTL	74LS368		DIP.16	P	HEX INV 2-4BT /3S	510974368
U9	INT-CKT	MLTVBRTR	9602			N	DUAL RETRIG/RESET	510096025
U10	INT-CKT	D/A-CONV	7523		DIP.16	N	8BT CMOS MULT	510100205
U11	INT-CKT	LS-TTL	74LS27		DIP.14	P	3X3 IN NOR GATE	510907427
U12-U13	INT-CKT	LS-TTL	74LS266		DIP.14	P	4X2 IN EX/NR GT O/C	510974266
U14-U15	INT-CKT	LS-TTL	74LS74		DIP.14	P	2 D POS EDG TRG F-F	510907474
U16	INT-CKT	COMPARTR	339		DIP.14	P	QUAD 5-36V	500000339
U17	INT-CKT	OP-AMP	1458		DIP.8	P	DUAL 741C	500001458
U18	INT-CKT	LS-TTL	74LS32		DIP.14	P	4X2 IN OR GATE	510907432
U19	INT-CKT	LS-TTL	74LS12		DIP.14	P	3X3 IN NAND GT /OC	510907412
U20	INT-CKT	LS-TTL	74LS10		DIP.14	P	3X3 IN NAND GATE	510907410
U21	INT-CKT	LS-TTL	74LS74		DIP.14	P	2 D POS EDG TRG F-F	510907474
U22	INT-CKT	LS-TTL	74LS14		DIP.14	P	HEX SCHMITT TRIGGER	510907414
U23	INT-CKT	LS-TTL	74LS266		DIP.14	P	4X2 IN EX/NR GT O/C	510974266
U24	INT-CKT	CMOS	4490		DIP.16	P	HX CNTCT BOUNC ELIM	510004490
U25	INT-CKT	VOLT-REG	7905		TO220	P	FIXED NEG 1.5A	500079050
XU3	SOCKET	PC MOUNT	40 DIL			N	.600 .180HT GOLD	820101400
XU7	SOCKET	PC MOUNT	40 DIL			N	.600 .180HT GOLD	820101400

TABLE 0

MEMORY AND TIMER (A2) PARTS LIST

A2760-11-019
REV 08 DATED 9/14/84

REFERENCE DESIGNATOR	DESCRIPTION					PART NO.
C1-4	CAPACITR ELECT-TA	22 UF	CAP.037	F	15V 10%	310002261
C5-18	CAPACITR CERAMIC	10 NF	CAP.082	F	16V 20% Y5P	330701031
C19	CAPACITR SIL-MICA	200 PF		F	500V 5%	335002010
C20-26	CAPACITR CERAMIC	10 NF	CAP.082	F	16V 20% Y5P	330701031
CR1	DIODE SIGNAL	1N4148	RES.001		75V SI 4.0NS	560041480
J1	CONNECTR HEADER	50 DIL			GOLD STRAIGHT	654003311
R1-3	RESISTOR CARBON	0.0 R	RES.001	P	1/4W ZEROHM	200100001
R4	RESISTOR MTL-FILM	1.00 K	RES.001	P	.25W 1% 100PPM 250V	220210011
R8-15	RESISTOR CARBON	2.2 K	RES.001	F	1/4W 10%	200102226
R16-18	RESISTOR CARBON	10 K	RES.001	F	1/4W 10%	200101036
U8	INT-CKT CMOS	5101L-1	DIP.22.4		256X4 BIT STATIC CM	514000406
U9	INT-CKT LS-TTL	74LS367	DIP.16	P	HEX BUF 2-4BT /3S	510974367
U10	INT-CKT MICRO-PR	8253			PROG INTERVAL TIMER	514001405
U11	INT-CKT LS-TTL	74LS14	DIP.14	P	HEX SCHMITT TRIGGER	510907414
U12	INT-CKT TTL	7432	DIP.14	N	4X2 IN OR GATE	510074320
U13-15	INT-CKT CMOS	5101L-1	DIP.22.4		256X4 BIT STATIC CM	514000406
U16	INT-CKT LS-TTL	74LS27	DIP.14	P	3X3 IN NOR GATE	510907427
U17	INT-CKT LS-TTL	74LS155	DIP.16	P	2X2TO4 DECDR/DEMUX	510974155
U18	INT-CKT LS-TTL	74LS20	DIP.14	P	2X4 IN NAND GATE	510907420
U19	INT-CKT LS-TTL	74LS125	DIP.14	P	4X3STATE BUS BUFFR	510974125
U20	INT-CKT LS-TTL	74LS00	DIP.14	P	4X2 IN NAND GATE	510907400
U21	INT-CKT LS-TTL	74LS156	DIP.16	P	2X2-4 DCDR/DMUX /OC	510974156
XU1-7	SOCKET PC MOUNT	24 DIL		N	.600 .180HT TIN	820101502
XU10	SOCKET PC MOUNT	24 DIL		N	.600 .180HT TIN	820101502

TABLE P

SINGLE FREQUENCY INPUT (A3) PARTS LIST

A2760-17-012
REV 08 DATED 9/14/84

REFERENCE DESIGNATOR	DESCRIPTION					PART NO.
C1-6	CAPACITR POLYPROP	27 NF	CAP.059	N	100V .5%	322902740
C7	CAPACITR ELECT-TA	1.0 UF	CAP.036	F	35V 20%	310901050
C8-10	CAPACITR CERAMIC	10 NF	CAP.088	F	50V 10% X7R	330801030
C11	CAPACITR CERAMIC	680 PF	CAP.082	N	1KV 10% Z5R	330006810
C12	CAPACITR ELECT-NP	4.7 UF	CAP.032	N	25V -10 +100% N-P	301304750
C13-14	CAPACITR POLYPROP	27 NF	CAP.059	N	100V .5%	322902740
C15	CAPACITR CERAMIC	680 PF	CAP.082	N	1KV 10% Z5R	330006810
C16	CAPACITR POLYESTR	180 NF	CAP.053	N	250V 10%	320218421
C17	CAPACITR CERAMIC	10 NF	CAP.088	F	50V 10% X7R	330801030
C101-106	CAPACITR POLYPROP	27 NF	CAP.059	N	100V .5%	322902740
C107	CAPACITR ELECT-TA	1.0 UF	CAP.036	F	35V 20%	310901050
C108-110	CAPACITR CERAMIC	10 NF	CAP.088	F	50V 10% X7R	330801030

TABLE P (Cont)

A2760-17-012
REV 08 DATED 9/14/84

REFERENCE DESIGNATOR	DESCRIPTION							PART NO.
C111	CAPACITR	CERAMIC	680	PF	CAP.082	N	1KV 10% Z5R	330006810
C112	CAPACITR	ELECT-NP	4.7	UF	CAP.032	N	25V -10 +100% N-P	301304750
C113-114	CAPACITR	POLYPROP	27	NF	CAP.059	N	100V .5%	322902740
C115	CAPACITR	CERAMIC	680	PF	CAP.082	N	1KV 10% Z5R	330006810
C116	CAPACITR	POLYESTR	180	NF	CAP.053	N	250V 10%	320218421
C117	CAPACITR	CERAMIC	10	NF	CAP.088	F	50V 10% X7R	330801030
C200-228	CAPACITR	CERAMIC	100	NF	CAP.088	F	50V 20% Z5U	330801040
C229	CAPACITR	CERAMIC	10	NF	CAP.082	F	16V 20% Y5P	330701031
C230-232	CAPACITR	ELECT-TA	10	UF	CAP.042	F	20V 20%	310801060
CR1-2	DIODE	SIGNAL	1N4148		RES.001		75V SI 4.0NS	560041480
CR101-102	DIODE	SIGNAL	1N4148		RES.001		75V SI 4.0NS	560041480
J1	CONNECTR	HEADER	17 SIL				R-ANGLE GOLD PC	654003119
J1A	CONNECTR	HEADER	17 SIL		CONN.1.1		GOLD R-ANGLE	654003219
R1-2	RESISTOR	MTL-FILM	9.25	K	RES.001	P	.25W 1% 100PPM 250V	220282511
R3-4	RESISTOR	MTL-FILM	1.30	K	RES.001	N	.25W 1% 100PPM 250V	220213011
R5	RESISTOR	MTL-FILM	10.0	K	RES.001	P	.25W 1% 100PPM 250V	220210021
R6	RESISTOR	MTL-FILM	9.53	K	RES.001	N	.25W 1% 100PPM 250V	220295311
R7	RESISTOR	MTL-FILM	9.09	K	RES.001	P	.25W 1% 100PPM 250V	220290911
R8	RESISTOR	MTL-FILM	1.02	K	RES.001	N	.25W 1% 100PPM 250V	220210211
R9	RESISTOR	MTL-FILM	10.2	K	RES.001	N	.25W 1% 100PPM 250V	220210221
R10	RESISTOR	MTL-FILM	402	K	RES.001	N	.25W 1% 100PPM 250V	220240231
R11	RESISTOR	MTL-FILM	20.0	K	RES.001	N	.25W 1% 100PPM 250V	220220021
R12	RESISTOR	MTL-FILM	2.15	K	RES.001	P	.25W 1% 100PPM 250V	220221511
R13-14	RESISTOR	MTL-FILM	2.26	K	RES.001	N	.25W.25%100PPM 250V	220422618
R15	RESISTOR	MTL-FILM	59.0	K	RES.001	N	.25W 1% 100PPM 250V	220259021
R17	RESISTOR	MTL-FILM	2.26	K	RES.001	N	.25W.25%100PPM 250V	220422618
R19	RESISTOR	MTL-FILM	18.2	K	RES.001	N	.25W 1% 100PPM 250V	220218221
R20	RESISTOR	MTL-FILM	9.09	K	RES.001	F	.25W 1% 100PPM 250V	220290911
R21-22	RESISTOR	MTL-FILM	18.2	K	RES.001	N	.25W 1% 100PPM 250V	220218221
R23	RESISTOR	MTL-FILM	9.09	K	RES.001	P	.25W 1% 100PPM 250V	220290911
R24	RESISTOR	MTL-FILM	22.1	K	RES.001	N	.25W 1% 100PPM 250V	220222121
R25	RESISTOR	MTL-FILM	4.64	K	RES.001	P	.25W 1% 100PPM 250V	220246411
R26	RESISTOR	MTL-FILM	10.0	K	RES.001	P	.25W 1% 100PPM 250V	220210021
R27	RESISTOR	MTL-FILM	18.7	K	RES.001	N	.25W 1% 100PPM 250V	220218721
R28	RESISTOR	MTL-FILM	54.9	K	RES.001	N	.25W 1% 100PPM 250V	220254921
R29-30	RESISTOR	MTL-FILM	3.01	K	RES.001	N	.25W 1% 100PPM 250V	220230111
R31	RESISTOR	MTL-FILM	2.26	K	RES.001	N	.25W.25%100PPM 250V	220422618
R32	RESISTOR	MTL-FILM	2.15	K	RES.001	P	.25W 1% 100PPM 250V	220221511
R33-35	RESISTOR	MTL-FILM	2.26	K	RES.001	N	.25W.25%100PPM 250V	220422618
R36-136	RESISTOR	MTL-FILM	24.3	K	RES.001	N	.25W 1% 100PPM 250V	220224321
R37	RESISTOR	MTL-FILM	6.98	K	RES.001	N	.25W 1% 100PPM 250V	220269811
R38	RESISTOR	MTL-FILM	1.00	K	RES.001	P	.25W 1% 100PPM 250V	220210011
R39	RESISTOR	MTL-FILM	590	R	RES.001	N	.25W 1% 100PPM 250V	220259001
R40	RESISTOR	MTL-FILM	1.00	K	RES.001	P	.25W 1% 100PPM 250V	220210011
R41	RESISTOR	MTL-FILM	590	R	RES.001	N	.25W 1% 100PPM 250V	220259001
R42	RESISTOR	MTL-FILM	2.00	K	RES.001	N	.25W 1% 100PPM 250V	220220011
R43-44	TRIM-POT	CERM-15T	200	R	VRES.001	F	3/4W 10% END-ADJ	232502010
R45	TRIM-POT	CERM-15T	20	K	VRES.001	F	3/4W 10% END-ADJ	232502030
R46	RESISTOR	MTL-FILM	100	R	RES.001	P	.25W 1% 100PPM 250V	220210001
R47	RESISTOR	MTL-FILM	3.01	K	RES.001	N	.25W 1% 100PPM 250V	220230111
R48	TRIM-POT	CERM-18T	5.0	K	VRES.010	P	1/2W 10% TOP-ADJ	232705025

TABLE P (Cont)

A2760-17-012
REV 08 DATED 9/14/84

REFERENCE DESIGNATOR	DESCRIPTION							PART NO.
R101-102	RESISTOR	MTL-FILM	8.25	K	RES.001	P	.25W 1% 100PPM 250V	220282511
R103-104	RESISTOR	MTL-FILM	1.30	K	RES.001	N	.25W 1% 100PPM 250V	220213011
R105	RESISTOR	MTL-FILM	10.0	K	RES.001	P	.25W 1% 100PPM 250V	220210021
R106	RESISTOR	MTL-FILM	9.53	K	RES.001	N	.25W 1% 100PPM 250V	220295311
R107	RESISTOR	MTL-FILM	9.09	K	RES.001	P	.25W 1% 100PPM 250V	220290911
R108	RESISTOR	MTL-FILM	1.02	K	RES.001	N	.25W 1% 100PPM 250V	220210211
R109	RESISTOR	MTL-FILM	10.2	K	RES.001	N	.25W 1% 100PPM 250V	220210221
R110	RESISTOR	MTL-FILM	402	K	RES.001	N	.25W 1% 100PPM 250V	220240231
R111	RESISTOR	MTL-FILM	20.0	K	RES.001	N	.25W 1% 100PPM 250V	220220021
R112	RESISTOR	MTL-FILM	2.15	K	RES.001	P	.25W 1% 100PPM 250V	220221511
R113-114	RESISTOR	MTL-FILM	2.26	K	RES.001	N	.25W.25%100PPM 250V	220422618
R115	RESISTOR	MTL-FILM	59.0	K	RES.001	N	.25W 1% 100PPM 250V	220259021
R117	RESISTOR	MTL-FILM	2.26	K	RES.001	N	.25W.25%100PPM 250V	220422618
R119	RESISTOR	MTL-FILM	18.2	K	RES.001	N	.25W 1% 100PPM 250V	220218221
R120	RESISTOR	MTL-FILM	9.09	K	RES.001	P	.25W 1% 100PPM 250V	220290911
R121-122	RESISTOR	MTL-FILM	18.2	K	RES.001	N	.25W 1% 100PPM 250V	220218221
R123	RESISTOR	MTL-FILM	9.09	K	RES.001	P	.25W 1% 100PPM 250V	220290911
R124	RESISTOR	MTL-FILM	22.1	K	RES.001	N	.25W 1% 100PPM 250V	220222121
R125	RESISTOR	MTL-FILM	4.64	K	RES.001	P	.25W 1% 100PPM 250V	220246411
R126	RESISTOR	MTL-FILM	10.0	K	RES.001	P	.25W 1% 100PPM 250V	220210021
R127	RESISTOR	MTL-FILM	18.7	K	RES.001	N	.25W 1% 100PPM 250V	220218721
R128	RESISTOR	MTL-FILM	54.9	K	RES.001	N	.25W 1% 100PPM 250V	220254921
R129-130	RESISTOR	MTL-FILM	3.01	K	RES.001	N	.25W 1% 100PPM 250V	220230111
R131	RESISTOR	MTL-FILM	2.26	K	RES.001	N	.25W.25%100PPM 250V	220422618
R132	RESISTOR	MTL-FILM	2.15	K	RES.001	P	.25W 1% 100PPM 250V	220221511
R133	RESISTOR	MTL-FILM	2.26	K	RES.001	N	.25W.25%100PPM 250V	220422618
R134-135	RESISTOR	MTL-FILM	2.26	K	RES.001	N	.25W.25%100PPM 250V	220422618
R137	RESISTOR	MTL-FILM	6.98	K	RES.001	N	.25W 1% 100PPM 250V	220269811
R138	RESISTOR	MTL-FILM	1.00	K	RES.001	P	.25W 1% 100PPM 250V	220210011
R139	RESISTOR	MTL-FILM	590	R	RES.001	N	.25W 1% 100PPM 250V	220259001
R140	RESISTOR	MTL-FILM	1.00	K	RES.001	P	.25W 1% 100PPM 250V	220210011
R141	RESISTOR	MTL-FILM	590	R	RES.001	N	.25W 1% 100PPM 250V	220259001
R142	RESISTOR	MTL-FILM	2.00	K	RES.001	N	.25W 1% 100PPM 250V	220220011
R143-144	TRIM-POT	CERM-15T	200	R	VRES.001	F	3/4W 10% END-ADJ	232502010
R145	TRIM-POT	CERM-15T	20	K	VRES.001	F	3/4W 10% END-ADJ	232502030
R146	RESISTOR	MTL-FILM	100	R	RES.001	P	.25W 1% 100PPM 250V	220210001
R147	RESISTOR	MTL-FILM	3.01	K	RES.001	N	.25W 1% 100PPM 250V	220230111
R148	TRIM-POT	CERM-18T	5.0	K	VRES.010	P	1/2W 10% TOP-ADJ	232705025
R200	RESISTOR	MTL-FILM	2.00	K	RES.001	N	.25W 1% 100PPM 250V	220220011
R201	RESISTOR	CARBON	1.0	K	RES.003	F	1/2W 10%	200201026
R202	RESISTOR	MTL-FILM	1.50	K	RES.001	N	.25W 1% 100PPM 250V	220215011
R203	RESISTOR	MTL-FILM	511	R	RES.001	P	.25W 1% 100PPM 250V	220251101
S1	SWITCH	TOGGLE	3PDT				ON-NONE-ON GOLD	620401200
U1-6	INT-CKT	OP-AMP	1458		DIP.8	P	DUAL 741C	500001458
U7-8	INT-CKT	RMS-CONV	536		DIP.14	N	DC OUTPUT	510100500
U9-10	INT-CKT	COMPARTR	311		DIP.8	N		500003111
U11	INT-CKT	CMOS	4011BUF		DIP.14	P	4X2 IN NAND GATE	510004011
U12-15	INT-CKT	OP-AMP	741		DIP.8	P	GEN PURPOSE	500007412
U16-17	INT-CKT	OP-AMP	1458		DIP.8	P	DUAL 741C	500001458
U18	INT-CKT	COMPARTR	339		DIP.14	P	QUAD 5-36V	500000339
U19	INT-CKT	TTL	7406		DIP.14	N	HEX INV BUF DRV /OC	510074060

9. GLOSSARY

A. General

9.01 This part defines the terms, abbreviations, and acronyms used in this publication.

"A" DIRECTION RECEIVER	Monitored SF address signaling appears on the mainframe DISPLAY A.
ADDRESS SIGNALING	Register signaling (called number)
"B" DIRECTION RECEIVER	Monitored SF address signaling appears on the mainframe DISPLAY B.
CCITT	Consultative Committee on International Telegraph and Telephone
CLR	Circuit Layout Record
CONTROLLED OUTPULSING	Used on trunks equipped for signaling integrity check. The originating office waits for a positive response from the called office before outpulsing. The two types of controlled outpulsing are: 1. Delay-Dial 2. Wink-Start
DELAY DIAL	A method of controlled outpulsing. The sequence is off-hook (Delay-Dial), on-hook (Start-Dial)
GLARE	Simultaneous seizure of a trunk from both ends. An off-hook signal from the called office of more than 500 msec is interpreted as a glare condition.
IDP	Interdigital period. Measured in milliseconds.
IMMEDIATE-DIAL OUTPULSING	Used on trunks not equipped for signaling integrity check. The originating office waits 150 to 210 msec after sending a connect (seizure) signal and then blindly outpulses.
LED	Light Emitting Diode
LINE SIGNALING	Supervision signaling (call status)
N	A one to four digit number which identifies specific violating pulses of a dialed digit
PPS	Pulses per second
REGISTER SIGNALING	Address signaling (called number)
SBL	Speed, % Break, Level Violation
SF	Single Frequency (2600 Hz)

SIGNALING INTEGRITY CHECK	Provides an indication of a trunk's ability to transmit signaling information. This test is made on a per-call basis by common control offices during the initial call setup. The two types of signaling integrity check are: 1. Delay-Dial or Wink-Start 2. Continuity and Polarity Check
START-DIAL	An on-hook signal following an off-hook from the called office.
SUPERVISION SIGNALING	Line signaling (call status)
TLP	Transmission Level Point. (The transmission level of any given point in a circuit expressed in dB as referenced to the 0TLP)
WINK-START	A method of controlled outpulsing. The sequence is on-hook, off-hook, on-hook. The off-hook portion is the "wink".
0TLP	The Zero Transmission Level Point. (An arbitrary reference point in a circuit from which all gains and losses are measured. Usually one end of the circuit)

northern telecom

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Northern Telecom Inc.

Network Support Systems Division
P.O. Box 649
Concord, New Hampshire 03301

Tel. (603) 224-6511
TWX 710-361-1886
Telex 94-3453